White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements Part II: Die-to-Die Interfaces

Industry Council on ESD Target Levels

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The Industry Council on ESD
http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association
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Abstract

This white paper on die-to-die (D2D) interfaces is an extension of the second revision of White Paper 2 on CDM target levels released in 2021. It addresses the need for a clear CDM target roadmap for D2D interfaces.

D2D interfaces are the central intellectual property (IP) blocks for a heterogeneous integration architecture. This heterogeneous integration technology, with several variants of 2.5D and 3D package integration schemes, is the key enabler for the continuation of Moore's law and will drive the growth of the semiconductor market in the coming years.

This white paper presents an industry-wide survey on the relevance of industry-aligned D2D CDM targets and the currently used targets for D2D interfaces. The survey results emphasize the need for a common roadmap.

The three main aspects of the paper are the assessment of the status of electrostatic discharge (ESD) control of the process steps with ESD exposure for D2D interfaces, the stress test approach, and the roadmap of the target values. These recommendations outline the tasks for the industry to get prepared for the use of high-density D2D interfaces in the years to come. The white paper affects IP design, chiplet design, foundry, and the outsourced semiconductor assembly and test (OSAT) industry as well as EDA vendors.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements on integrated circuit (IC) products for safe handling and mounting in ESD-protected areas while addressing the constraints from silicon technology scaling and IC design. The Council now consists of representatives from active full-member companies and numerous associate members from various support companies.

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Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD-protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for future ESD target levels. The Council Members and Associates will promote these recommended targets for adoption as company goals. As an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Preface

This document is targeting the need to align the ESD target levels for D2D interfaces used in heterogeneous integrated components. Due to the exploding number of interfaces per package, the ESD protection design is limited to a minimum area and power consumption of the protection circuit per D2D I/O. This inevitably commands a reduction in the ESD robustness targets of these D2D interfaces to significantly lower levels than for external package balls. Nevertheless, protection design targets and manufacturing capabilities need to be well aligned to guarantee safe production. A careful assessment and optimization of the 2.5D/3D assembly manufacturing line for the process steps with exposure of the D2D interfaces to potential discharge events are required. This document will provide guidance for the robustness of the D2D interfaces in the forthcoming product generations for the development of ESD control programs that comply with the low robustness of the components. Additionally, it addresses the challenge of an appropriate qualification test methodology as standard CDM testing becomes impractical for an extremely high number of interfaces with very small µballs or hybrid bond pitch.

In a nutshell, this document attempts to synchronize the activities of ESD control in manufacturing, IP design of D2D interfaces, product ESD protection design, electronic design automation (EDA) vendors, and ESD test tool suppliers in preparing for the challenges of heterogeneous integrated systems.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies and contract manufacturers.

<u>The Industry Council, while providing these recommendations, does not assume any liability or obligations for parties who do not follow proper ESD control measures.</u>

Glossary of Terms

ANSI	American National Standards Institute
cc-TLP	capacitively-coupled transmission line pulse
CDM	charged device model
CoW	chip-on-wafer
CoWoS®	chip-on-wafer-on-substrate
D2D	die-to-die
DOE	design of experiments
EDA	electronic design automation
EOS	electrical overstress
ESD	electrostatic discharge
ESDS	ESD-sensitive
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association
FA	failure analysis
FICDM	field-induced charged device model
FINFET	fin field-effect transistor
FPGA	field-programmable gate array
FWHM	full-width half maximum
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
HBM	high bandwidth memory
HBM	human body model
HVM	high-volume manufacturing
IC	integrated circuit
IDM	integrated device manufacturer
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
InFO	integrated fan-out
IP	intellectual property
I/O	input/output
JEDEC	JEDEC Solid State Technology Association
LICCDM	low-impedance contact charged device model
LSI	local silicon interconnect
MCP	multichip package
MIM	metal-insulator-metal
OSAT	outsourced semiconductor assembly and test
PDK	process design kit
RC	resistor-capacitor network
RDL	redistribution layer
SoC	system-on-chip
UCIe™	Universal Chiplet Interconnect Express
VF-TLP	very-fast transmission line pulsing
$V_{charging}$	the charging voltage in a real-world scenario
V_{CDM}	charging voltage of field plate in CDM test setup
W2W	wafer-to-wafer
WoW	wafer-on-wafer

system-on-chip (SoC): Throughout this white paper, the term will commonly be used to refer to any 2.5D or 3D multi-chip package (MCP) or multi-chip module that contains D2D interconnects.

Executive Summary

This document addresses the targets of electrostatic discharge (ESD) design, manufacturing control, and testing for die-to-die (D2D) interconnects, **which is exclusively a topic for IC assembly and testing of chiplets by OSATs, foundries, or IDMs.** Once the chiplets are assembled in a package these die-to-die interfaces are no longer exposed to ESD risk.

For this purpose, an industry-wide survey of requirements and targets for D2D interfaces has been performed. More than 60 responses across industry and geographic locations were collected. It shows the high relevance and urgency of the topic. The need for standardization of the charged device model (CDM) design goals as well as the manufacturing assessment was clearly expressed.

It should be noted that throughout this white paper, the term system-on-chip (SoC) will commonly be used to refer to any 2.5D or 3D multi-chip package (MCP) or multi-chip module that contains D2D interconnects.

This paper is the foundation for the standard intellectual property (IP) development of D2D hard IP. Area and power constraints enforce an unprecedented lowering of the CDM requirements for D2D interfaces to 5 V for products starting as early as volume production in 2024. The implementation of the required ESD control is anticipated to occur in steps. While a few lead assembly sites equipped for advanced heterogeneous integration are already prepared for the lower-level ESD robustness of D2D interfaces, others in the industry might take a couple of years to comply with the requirements. This is indicated in the graph in the time frame from 2024 to 2028. It is also anticipated that another transition to 3 V beyond 2028 for high-density D2D interfaces with even tighter bump pitches (see Figure 1) will be needed.

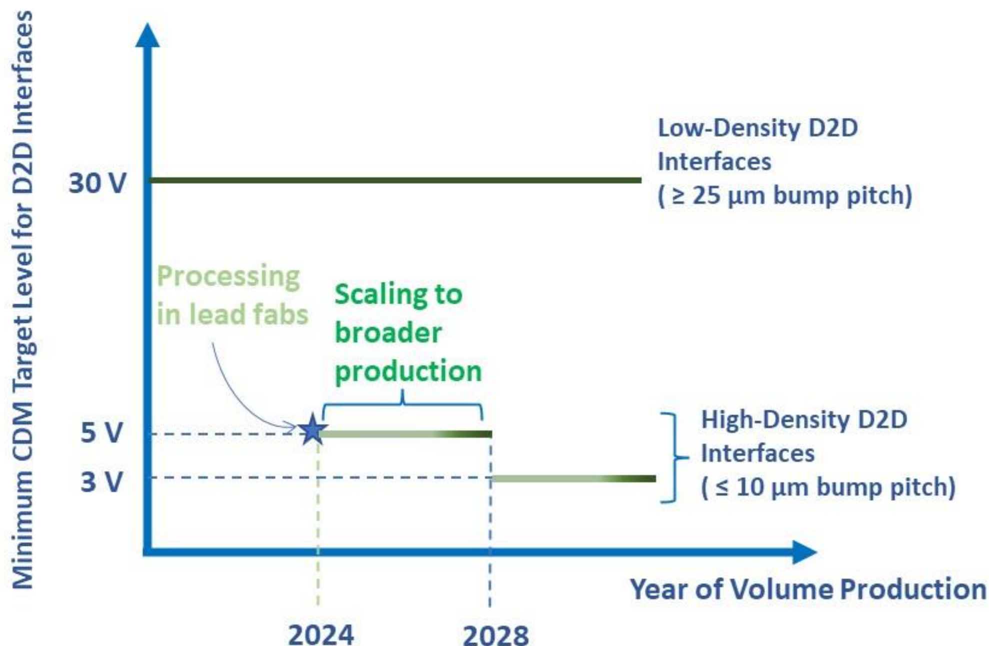

Figure 1: Roadmap of CDM Targets of Die-to-Die Interfaces

IP development must be related to CDM peak current. The peak current depends on the size of the die. Reference values of 75 mA to 116 mA are given for a 5 V target assuming typical die sizes from 60 mm^2 to 500 mm^2. This reduces to 45 mA to 70 mA for a 3 V CDM target. The actual peak current values depend on the capacitance of the die to the charging plate in the CDM test setup and the discharge impedance. The actual capacitance of the die is typically lower, but this requires additional investigation, determining this actual capacitance, and thus peak current, is essential to determine the optimum design solution.

To guarantee the safe manufacturing of components with low-level CDM D2D interfaces, a detailed process assessment must be performed of the process steps before and up to the point where wafers are bonded, die are bonded to a wafer, or die are attached to a package substrate (with or without D2D bridges). At this point, it is presumed the D2D interface is no longer exposed to an ESD risk. This is specific to each assembly process variant. American National Standards Institute (ANSI)/ESD SP17.1 describes methodologies to assess manufacturing facilities at low charging and discharging levels. Based on survey responses, it is felt that more information than is contained in ANSI/ESD SP17.1 is needed, but it should be noted that this will be difficult if not impossible to do. At these low target levels, critical process assessments must be completed on the tools used to handle die/wafers. There are no shortcuts based on a simple list of things to do. As these tools will vary from company to company, an ESD expert must leverage the process assessment techniques as discussed in ANSI/SP17.1 for assessing these tools. Even if the tool is of the same type, there may be differences in materials used or the process itself that could influence the charging or discharging risk. Assessment of materials that may contact these die/wafers is no different from what is discussed in ANSI/ESD S20.20.

Standard field-induced CDM testing of the chiplets according to ANSI/ESDA/JEDEC JS-002 does not apply to high-density D2D interfaces for three reasons:

- ANSI/ESDA/JEDEC JS-002 field-induced CDM (FICDM) testing gives meaningless results in the sub-100 V range.
- The tighter pitch (~10 µm and down to 1 µm in the future) is beyond the capabilities of today's most advanced systems.
- The high number of hybrid bonds or µbumps, which can be hundreds to millions, is beyond the scope of reasonable testing.

Fortunately, the overwhelming majority of D2D interfaces are exact copies of a few standard input/output (I/O) variants. The following approaches are therefore proposed:

- Perform the stress test on a test vehicle that contains the set of D2D interface variants.
- Include the design for test measurement capability for the SoC by providing contact points for a few representative D2D interfaces covering the used D2D interface variants.

The stress test can be executed using very-fast transmission line pulse (VF-TLP), capacitively-coupled TLP (cc-TLP), or low-impedance contact CDM (LICCDM) testing. A stress test of

the D2D interfaces on the SoC is not required if a comprehensive test of the IP on a test chip has been performed.

During the sign-off, the verification tools must validate the correct integration of the D2D interface cells. Full coverage of all D2D I/Os must be guaranteed. This is especially critical because a later ESD qualification test on the D2D I/Os on a fully assembled SoC is not possible.

In summary, a call to the industry is presented to prepare for low-level CDM robustness of D2D interfaces to account for area and power constraints. This opens the door for the wide use of D2D interfaces and, consequently, to the full capability of heterogeneous integration.

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Chapter 1: Overview of Heterogeneous Integration Technology

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1.1 Introduction to Heterogeneous Integration

Heterogeneous integration is an assembly technology to integrate chiplets of similar (like memories) or diverse (like digital and analog) functions into one package. This realizes a much higher packing density and lowers the power consumption due to shorter interconnects (Figure 2).

There are various types of heterogeneous integration schemes in use [Wu2021]. This includes wafer-on-wafer (WoW) and chip-on-wafer (CoW) process variants as shown in Figures 3 and 4. The stacking schemes entail 2.5D and 3D stacking. Silicon, glass, and organic interposers are applied in 2.5D technologies. In addition, the organic interposer technology allows one to choose between a chip first or a chip last configuration in various implementations (Figure 5 and Figure 6) where a silicon interposer represents a more traditional lateral die communication in the metal routing in silicon and a redistribution layer (RDL) interposer has the lateral die communications routed in the RDL. The metal connections between the dies are implemented as µbumps based on traditional solder bump technology or hybrid bonding with Cu-Cu connections. The 3D wafer stack can be found either as front-to-front or front-to-back configurations as shown in Figure 7. The different process variants create different exposure of D2D interfaces to ESD and have to be assessed individually. This requires detailed knowledge of the process and its effect on ESD. A general description of assessment methods is given in ANSI/ESD SP17.1. The aspects of a specific analysis of the D2D relevant process steps are discussed in Chapter 3.

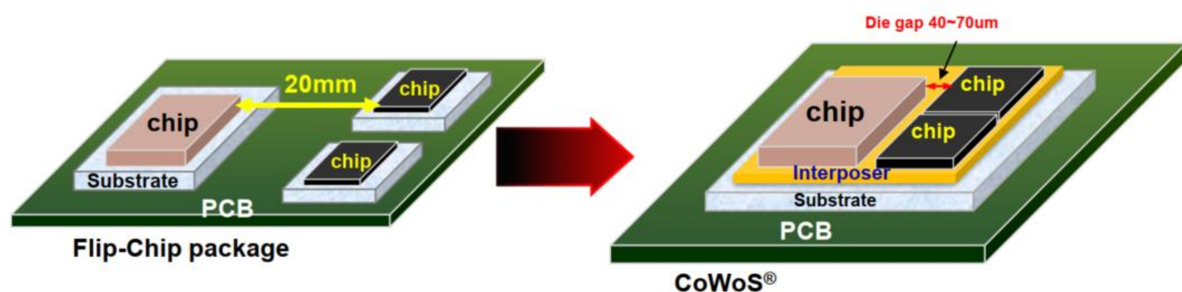


Figure 2: 2.5D Chiplet Integration on an Interposer

Note: This reduces the wiring length between the chiplets and enables a higher integration density.

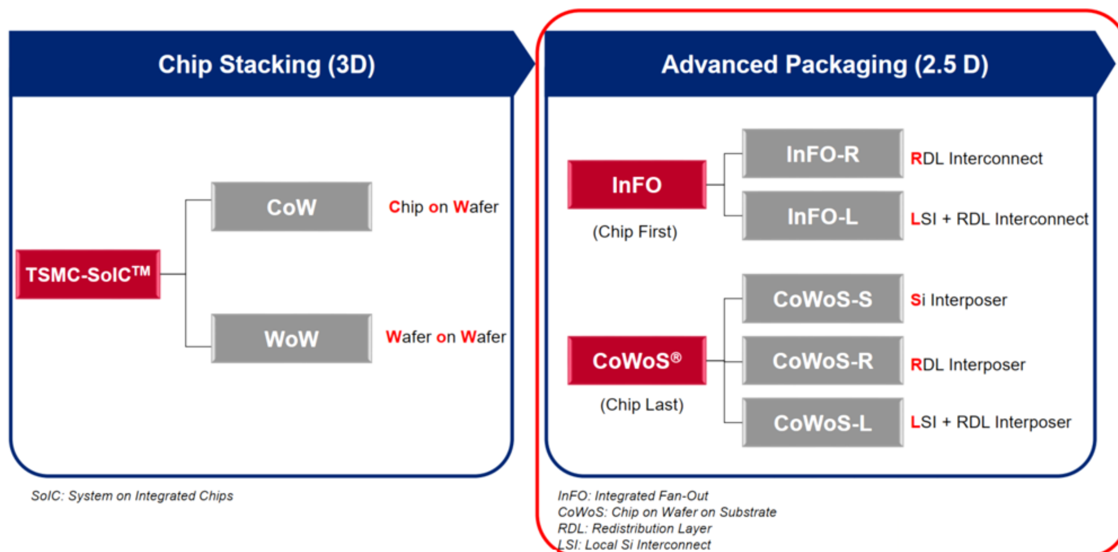


Figure 3: Various Types of 3D and 2.5D Integration Schemes

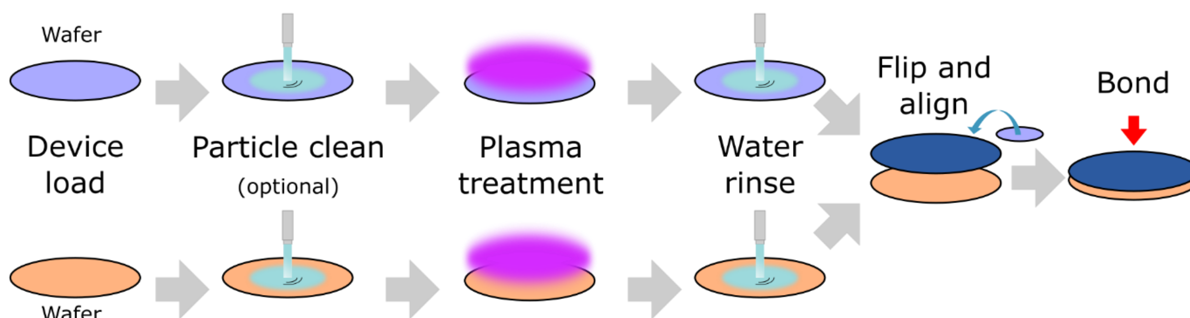


Figure 4: Schematic of the Wafer-to-Wafer Hybrid Bonding Process

Note: Two wafers are loaded into the bonding tool. Both wafers undergo a plasma treatment to activate the dielectric. One wafer is flipped without touching the front side. All dies are collectively bonded in a single bonding step.

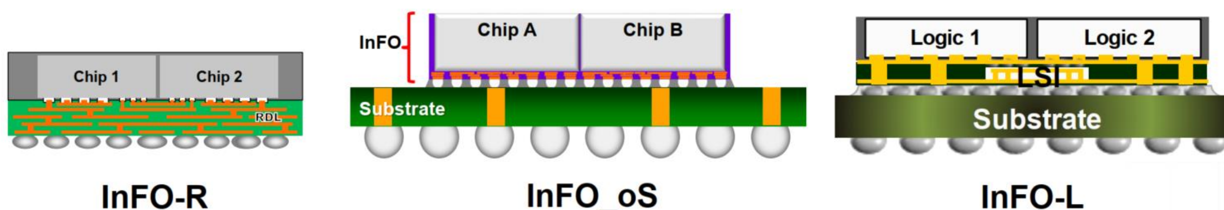


Figure 5: Cross Section of Various 2.5D Integration Schemes w/o Interposer

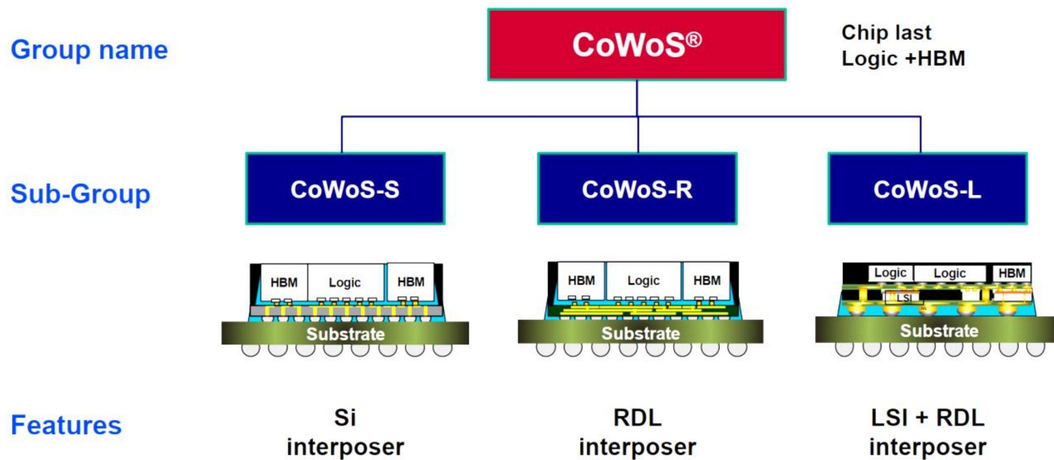


Figure 6: Various Interposer Technologies

Note: RDL = redistribution layer, HBM = high bandwidth memory, LSI = local silicon interconnect

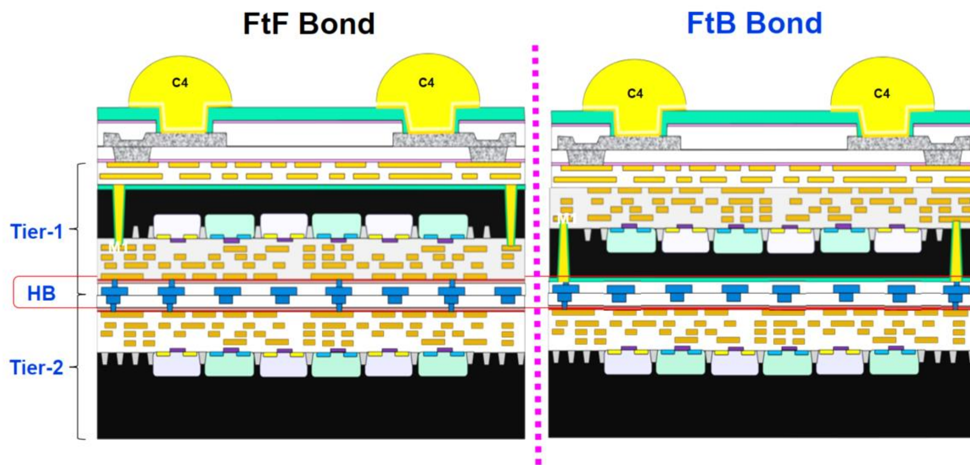


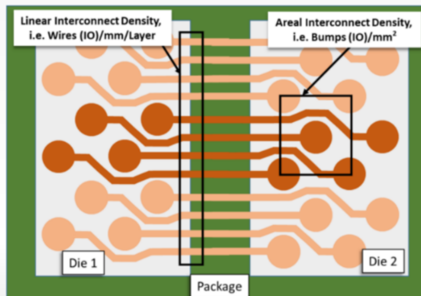
Figure 7: Hybrid Bonding a) Front-to-Front b) Front-to-Back

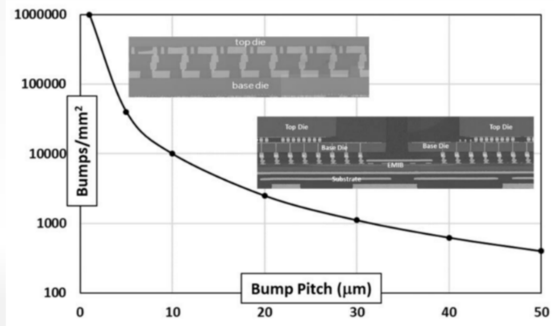
1.2 Roadmap of µbumping and Hybrid Bonding

The number of D2D interfaces is predicted to increase exponentially in the coming years. Thousands and even millions of D2D interconnect may be found in heterogeneous integration systems soon. It is expected that the interconnect pitch will drop below 10 µm in the next 2-3 years, making direct probing for TLP evaluations nearly impossible. Research and development work has shown a hybrid bond pitch of less than 1 µm as shown in Figure 8.

Vertical Interconnects : MCP Landscape

Transition from Solder Based Interconnects to Cu-Cu interconnects needed with shrinking Bump Pitch*





*Li et al. "Scaling Solder Micro-Bump Interconnect Down to 10 µm Pitch for Advanced 3D IC Packages" ECTC 2021

intel. 11

Figure 8: Multi-Chip Package Landscape

1.3 Impact of ESD Protection Design of D2D Interfaces on Power, Performance, Area, and Cost

A typical dual diode protection concept in a fin field-effect transistor (FINFET) technology has a footprint of 0.05 - 0.1 $\mu m^2/mA$ and a capacitive load due to ESD protection of ~0.1 fF/mA. For example, a CDM target level of 35 V results in typical CDM peak currents of 150 mA - 300 mA depending on the size of the die. For a million D2D interfaces, the ESD-related area amounts to 8 mm^2 - 30 mm^2 of chip area. The capacitive load of 15 - 30 nF leads to excessive power consumption. This needs to be accounted for in the specification of a CDM target level.

Chapter 2: Industry Survey on ESD Targets of Die-to-Die Interfaces

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2.1 Set-up of Survey

The industry survey was designed by the working group focused on D2D interfaces for the Industry Council on ESD Target Levels. The survey was launched at the beginning of June 2022. The information presented here in this document results from the industry feedback collected after the survey ended in November 2022.

The survey addresses the need for specific CDM targets for D2D interfaces and dedicated ESD control measures for the heterogeneous integration process. In total, 30 questions were asked, either single-choice, multiple-choice, or text-based. The questionnaire could be completed leaving any number of questions unanswered. Answers left blank were ignored for the analysis. All questions for the survey are shown in Appendix A and results are shown in Appendix B.

Some of the answers given in text form have been paraphrased, and/or similar ones combined for the data presented in Section 2.3 and Appendix B.

2.2 Analytics of Participation

57 responses were received from the survey, spanning the Americas, East Asia, and Europe [Q02]. The responses came from a wide range of industries including silicon foundries, integrated device manufacturers (IDM), design houses, IP vendors, outsourced semiconductor assembly and test facilities (OSATs), contract manufacturers, and electronic systems manufacturers [Q01, Q03].

2.3 Trends and Conclusions

This section will discuss the results of the survey starting with ESD design targets followed by ESD control standards for D2D processes.

2.3.1 ESD Design Targets for D2D Interfaces

- 51% of all respondents apply lower CDM targets for D2D than for external balls, while 25% don't apply lower targets for D2D interfaces. 24% indicated that it doesn't apply to them [Q04]. A majority of those who don't apply a D2D process in their workflow are e.g., system manufacturers, failure analysis (FA) labs, or distributors.

  In some cases, different experts from the same company provided both the answer of reduced and non-reduced targets. This might depend on the types of products or designs they are addressing.

This means that 2/3 of the respondents who are exposed to the challenge of D2D interface design or processing, apply lowered targets. 1/3 of the respondents don’t. It is suspected that their products only contain a low number of D2D interfaces, and the impact of the area does not affect the SoC design critically.

- 32% of all respondents apply different CDM targets for D2D depending on whether it is a 2.5D or 3D process [Q05]. A clear trend towards this practice is observed for foundries whereas the responses vary for the other sectors.

- 56% of all respondents see a need to lower the targets to satisfy the power, performance, and area requirements for future products [Q08]. Considering that 28% answered that the question doesn´t apply to them, this means that 78% of the respondents that are exposed to the challenge of D2D interface design are looking into lowering the targets to meet critical product key performance indicators.

- 79% of all respondents see a need for an industry alignment on target levels [Q09]. As compared to previous questions, only a small group of 9% selected “n/a”, indicating that even the companies not directly dealing with D2D interface designs and processes are in favor of an industry alignment.

- The currently applied target levels are widely spread and vary from 3 V to > 70 V or 10 mA to > 300 mA, respectively [Q11, Q12, Q13]. Possible explanations for the wide range of targets are:
    - correlation to the 2.5D and 3D hybrid bonding type of heterogeneous integration technology [Q05] as well as differing number and density of 2.5D and 3D interconnects for different product designs,
    - missing standards in the industry [Q09, Q10] and missing knowledge of manufacturing capabilities and limitations [Q21 – Q24, Q29, Q30],
    - limited experience with actual D2D fail limits, i.e., product/high-volume manufacturing (HVM) fails or design of experiments (DOEs) in production as can be seen from the responses to questions [Q17 – Q24],
    - different robustness levels of technology nodes,
    - different needs and pain points for different types of designs; different customer requests [Q12, Q13].

- A similar diversity is found for the implementation of ESD protection (diodes, local clamps, self-protection, or a combination thereof) [Q14, Q15], as well as the verification (simulation, static layout verification, silicon-data based, …) of the D2D ESD protection [Q06, Q07].

- 48% of all respondents are detailing a timeline for products with reduced D2D targets going into volume production. Out of these, 44% report this taking place as early as 2022, and another 41% by 2024 [Q16].

Based on these responses, it can be concluded that dedicated D2D targets are relevant for design and standardization and are highly desired with 74% of respondents asking for a robustness target specified in current [Q25]. The product roadmap schedules illustrate the urgency of an alignment

in the industry. However, the variety of currently applied targets and approaches presents a challenge for design and manufacturing to align on common metrics for success.

2.3.2 ESD Control Standards for D2D Processes

- 88% of all respondents see the need for ESD control standards [Q10], representing the broadest agreement to any question in this survey.

- 24% of respondents who answer the question stated that they have encountered ESD fails on D2D interfaces [Q17] with some of them having experienced them in more than one place. Of all detected fails, 73% of them were detected in HVM testing, 20% at the customer, and in one case (6%) at system level testing [Q18]. 38% of the observed failures could not be root caused while 23% occurred during testing and 15% during die stacking [Q19].

- The feedback on what is considered a minimum safe level from a manufacturing perspective varies over a large range from 3 V to 200 V [Q20]. Yet only 18% of the relevant responses state that experiments have been carried out to establish a safe manufacturing target (1 for 3 V, 1 for 5 V, 3 for 10 V target, 1 for 30 V target, 1 for 200 V) [Q21]. DOEs are mostly based on CDM or transmission line pulse testing to determine the D2D robustness, sometimes at different production levels [Q22]. Only two responses stated that DOEs with different D2D protection variants were carried out [Q22]. This is a testimony to the effort associated with this type of investigation. In the cases where experiments were conducted, the achievable max voltage limit in production environments is stated to be from 3 V to 70 V, and in one case to meet to S20.20-2014 standard, again showing a notable spread [Q23]. In two cases the achievable max voltage limit in the production environment is reported to be larger than the minimum safe voltage level stated in [Q20]. This would imply a risk of damage to the D2D interface.

  Only one company claims that a discharge current can be measured directly in the manufacturing environment [Q24].

  18 companies that provided safe CDM target levels for manufacturing also responded that they haven’t executed any experiments [Q02, Q21]. The choice of the level can be based on information from a 3rd party, or customer request, or might be driven by a ‘best I can do’ design approach.

- Document-based ESD risk assessment: 54% of all respondents perform an ESD risk assessment of production lines, whereas only 14% don´t. 32% state that the question doesn´t apply to them [Q26]. The most relevant document is ANSI/ESD S20.20 which is used for 51% of all assessments. Proprietary internal documents are the second most applied with 26% [Q27]. Many make use of multiple documents for their assessments. Frequencies for assessments vary, sometimes on a fixed cycle, sometimes for the introduction of new products, and sometimes on a need basis [Q28].

ANSI/ESD SP17.1 as a document for ESD process assessment seems to be sufficient for D2D purposes for 21% of all respondents (whereas 62% responded with “n/a”) and only 13% listed it as being used in their assessment [Q29]. Multiple proposals on how to improve the documents were made [Q30].

While the stated values on the minimum safe levels vary over a large range, only a minority of the respondents have backed them up with their experimental data. Yet, an overwhelming majority, 88% of all respondents, have expressed the wish for an ESD control standard for D2D processes [Q10].

But while the survey request has asked for this control standard, it should be noted that this will be difficult to go beyond today’s documents like ANSI/ESD SP17.1 and ANSI/ESD S20.20 documents. At these low target levels, critical process assessments must be completed on the tools used to handle die/wafers. As these tools will vary from company to company, an ESD expert can leverage the process assessment techniques as discussed in ANSI/SP17.1 for assessing these tools. Assessment of materials that may contact these die/wafers are no different from what is already discussed in ANSI/ESD S20.20 but are also critical in the ESD risk assessment. This is a call for action for standardization bodies like the ESDA to address this problem by improving education in this area.

Chapter 3: Process Control

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3.1 Application of Existing Standards

Current ESD control standards claim safe handling of devices with a minimum CDM robustness of 200 V. These are ANSI/ESD S20.20, International Electrotechnical Commission (IEC) 61340-5-1, and JEDEC Solid State Technology Association (JEDEC) JESD625. Next to general ESD protection measures like operator grounding and requirements for chairs, worksurfaces, etc., they describe requirements for process-related insulators. Unfortunately, they do not give much guidance for assessing the risk inside automated handling equipment, where the devices might get charged by the process itself.

The recently released standard practice ANSI/ESD SP17.1 "Process Assessment Techniques" describes a set of methodologies, techniques, and tools that can be used to characterize processes where ESD-sensitive (ESDS) items are handled. The process assessment covers risks by charged personnel, ungrounded conductors, charged ESDS items, and ESDS items in an electrostatic field. Using the described measurement techniques, it is possible to determine whether sensitive devices can be handled in a process without risk from ESD damage. However, only highly experienced ESD control engineers are skilled enough to apply these techniques correctly and with accuracy. Even then it is very difficult to compare the charging voltage values measured in production with the stress voltage applied during ESD qualification testing.

Therefore, it would be much better to compare the stress currents observed during qualification with the currents observed during the actual ESD events in production. Such a technique was already successfully applied ([Gae2014], [Nie2016]) but it is not used often during the assessment, yet.

For any ESD control measurement method with automated handling equipment, the process always has to be interrupted. That could result in a reduction of the actual charging value until the measurement could be started. These measurement methods also do not tell whether there is a discharge, they just give information regarding the risk if there would be an ESD event. Therefore, it would be better to use techniques that do not interrupt the process and that can detect if a discharge occurs. Techniques, where the electromagnetic radiation of an ESD event is measured, could help here. First reports ([Mar2001], [Tam2017]) show that this is possible for detection. More recent evaluations ([Vih2022], [Zei2021]) show that even the corresponding current waveforms of the discharge can be determined when fully characterized antennas are used. Of course, these techniques have to be further evaluated.

3.2 Need for Standards

There is no standard available that describes the requirement for ESD protective measures needed in a production line for products with a low CDM robustness of D2D interfaces. The survey clearly shows that there is a widely perceived need to get such a standard. Especially when scaling the production capability of 2.5D and 3D to OSAT. But a standard with defined requirements in the form of a checklist cannot be provided. Every description would just be valid for one specific process step with one specific tool. Even if the tool is of the same type there might be differences in materials used or the process itself that could influence the charging or discharging risk. Therefore, it is much better to utilize the measurement techniques/methods as described in ANSI/ESD SP17.1 to complete the necessary risk assessment. With ANSI/ESD SP17.1 techniques/methods, engineering judgment and experience are needed to assess the possible ESD risk in the respective process.

3.3 Risk Analysis & Dependency of Different Process Routes

For processes before bonding (including the application of redistribution layers), the ESD risk is the same as with a "normal" die. Human body model (HBM) is not an issue for D2D assembly processes while the sensitivity of die to CDM, as well as to stress scenarios not described by the classical qualification targets but due to static discharges (e.g., during cleaning after dicing or similar), might be higher. The ESD risk for the bonding processes is described in more detail below.

3.3.1 Defining the Process Critical Path

When the dies are bonded with wires there is a risk of a hard discharge if the die is charged when the grounded wire makes contact with the pad. The first contact would discharge the contacted die and makes the chip neutral for the rest of the contacts. Therefore, it is always a good practice to bond to a less sensitive pad, such as ground, first.

3.3.2 Die-to-Die Bonding

We expect that the ESD risk during D2D assembly is similar to a die-to-wafer assembly process and will not be discussed further in this white paper.

3.3.3 Die-to-Wafer Bonding

<u>Discharge during picking</u>

The die is picked up with a suction cup from the dicing tape (sawing foil) making contact on the top side of the die.

No discharge from the die to the handling tool will be possible if the die is not charged. The charging of the die might be controlled by ionization or by a dissipative dicing tape but very often it is difficult or impossible to install the ionizer in a way that the ions reach the charged dies without being blocked by any equipment parts (shadowing effects). Additionally, the ionizer might be fast enough to discharge the dies before picking but might not be fast enough to neutralize the charges on the die after picking (during contact and separation charge is generated). Another possibility might be the use of a dissipative dicing tape to dissipate the charges on the die. An ESD event might happen if the die is charged before picking and the suction cup for picking is made of a very conductive material (metal). Additionally, the pickup nozzle must be grounded to avoid

accumulating charges that can be discharged into the die to be picked up. The best way to reduce all these risks would be to use a dissipative grounded suction cup.

The ESD critical process of picking and placing in a die-to-die or die-to-wafer process is shown in Figure 9 and Figure 10.

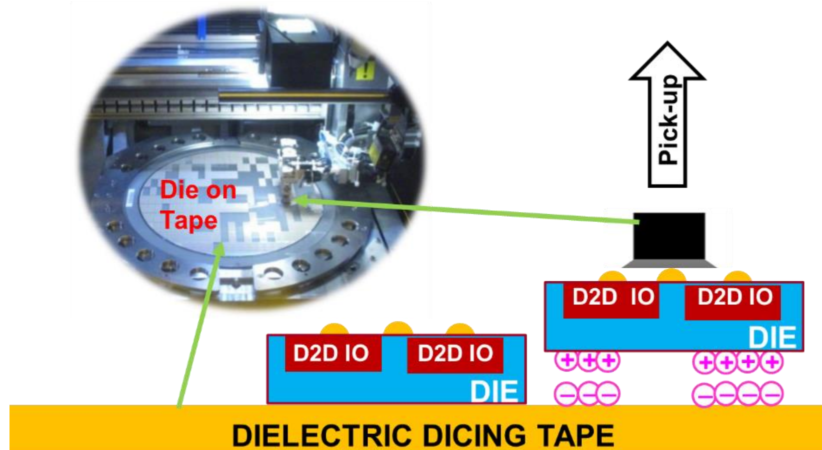

Figure 9: Charging Process During Die Assembly

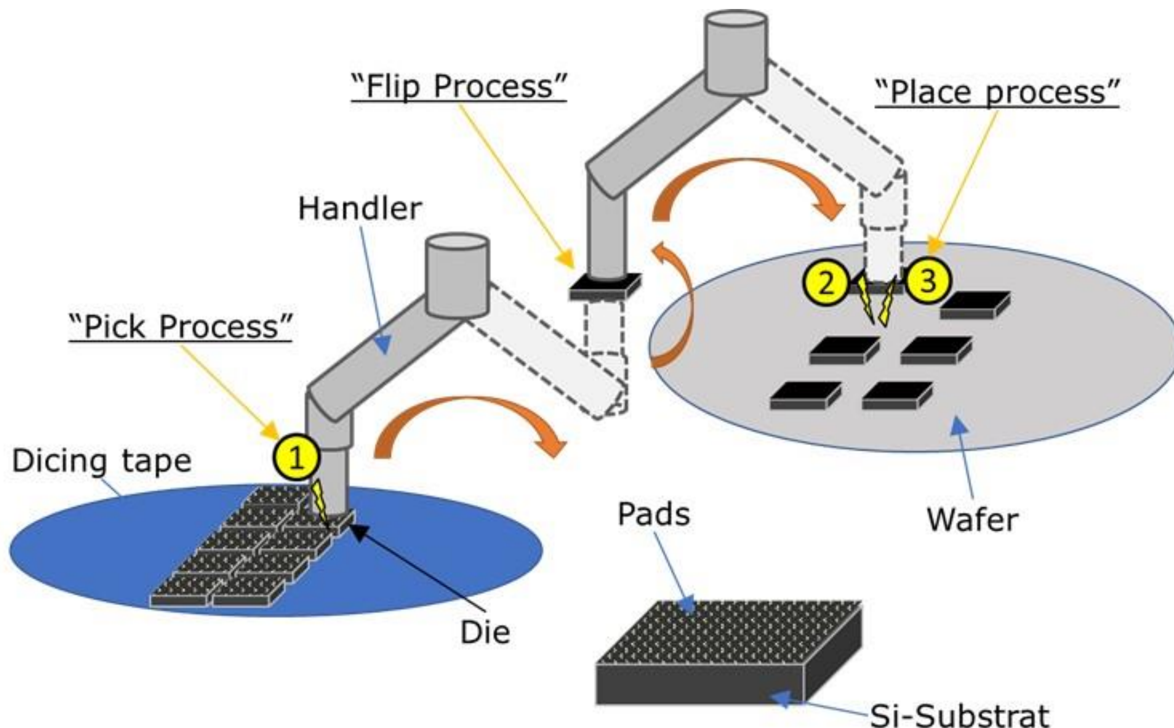

Figure 10: Discharging Risk During Die-to-Wafer Assembly

As can be seen in Figure 9, the die will get charged up when picked from the dicing tape. Figure 10 shows the three different risks that may exist until the die is placed on the bottom wafer.

1) Pick process: The handler contacts the die on the pad side (1).
    a. If the die on the dicing tape is still charged and the picking tool is very conductive (e.g., metallic) a CDM-type of discharge might happen.
    b. If the die on the dicing tape is still charged and the picking tool is dissipative, a controlled discharge with a low current will happen.
    c. If the die on the dicing tape is still charged and the picking tool is insulative no discharge will happen, but the die might still be charged at the next process step.
2) Flip process: The second handler arm contacts the die on the backside of the die.
    a. If the die is not charged no discharge will happen independent of the material of the second picker.
    b. If the die is charged and the second picker is made of conductive or dissipative material the die will not be charged at the next process step; even if the second picker is metallic the discharge will nevertheless happen through the silicon substrate with a much smaller current density and the die is not at risk.
    c. If the die is charged and the second picker is made of insulative material no discharge will happen and the die will still be charged at the next process step.
3) Place process: The die is placed onto the bottom wafer with the pads facing downwards.
    a. If the die is still charged it can discharge into the bottom wafer if the bottom wafer is at a different potential (CDM-like event (2)).
    b. If the die is not charged but the bottom wafer is charged the bottom wafer is discharging into the top die (inversed CDM-like event (3)).

A similar scenario is also described in Figure 11, after picking, the die is handed over to the bonding nozzle, which makes contact on the backside. If the die is charged coming from the pickup suction cup and the bonding suction cup is conductive/dissipative the die will be discharged via the bonding suction cup in a controlled way. This discharge via the die backside is typically not critical.

If the die is charged coming from the pickup suction cup and the bonding suction is insulative, then the die will not be discharged and can discharge when placed onto the wafer (die to wafer discharge). Every single die can be charged and discharged into the wafer. The best way to reduce these risks would be to use a conductive/dissipative material for the bonding suction cup and electrically ground it.

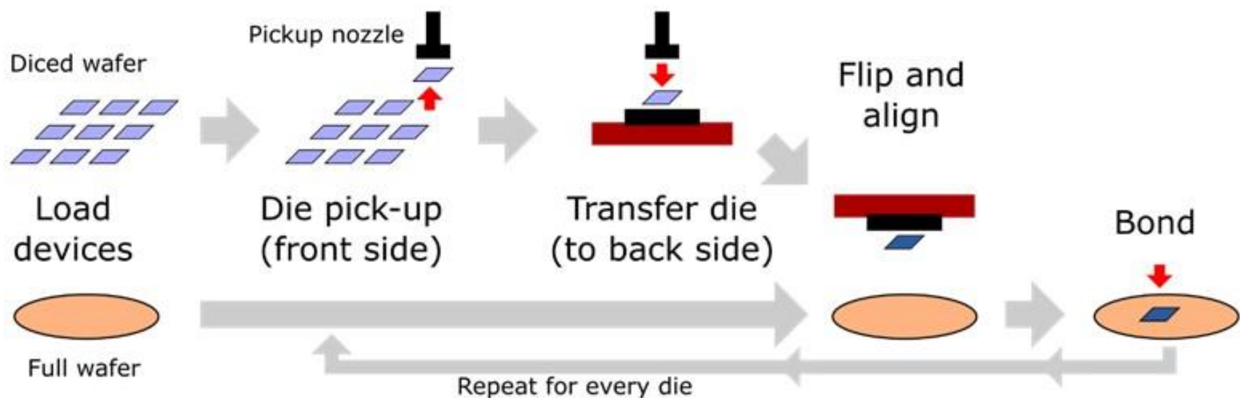

Figure 11: Schematic of the Die-to-Wafer Micro-bump Bonding Process
Note: One wafer and multiple dies are loaded into the bonding tool. The bonding process is repeated for every die until all necessary dies have been bonded to the wafer.

3.3.4 Wafer-to-Wafer Bonding

The wafer-to-wafer bonding process is depicted in Figure 12 to Figure 14. When a complete wafer is bonded onto another wafer at a different potential the discharge only happens once, and all the charges are flowing via one connection typically in one die. The techniques to get rid of the charges are the same as with die-to-wafer bonding but there is no picking of a single die from a foil and therefore less triboelectric charge generation. Additionally, ionization might be more effective since the ions might reach at least one part of the wafer to reduce the voltage on the wafer. However, these assumptions might change from technology to technology. For example, dies made in a silicon-on-insulator technology might be better isolated from each other, and therefore a discharge of one die might not mean the whole wafer is discharged. The same might be true for a thinned wafer on a glass carrier. Care must be taken here to understand the technology-specific risks and apply specific solutions if needed.

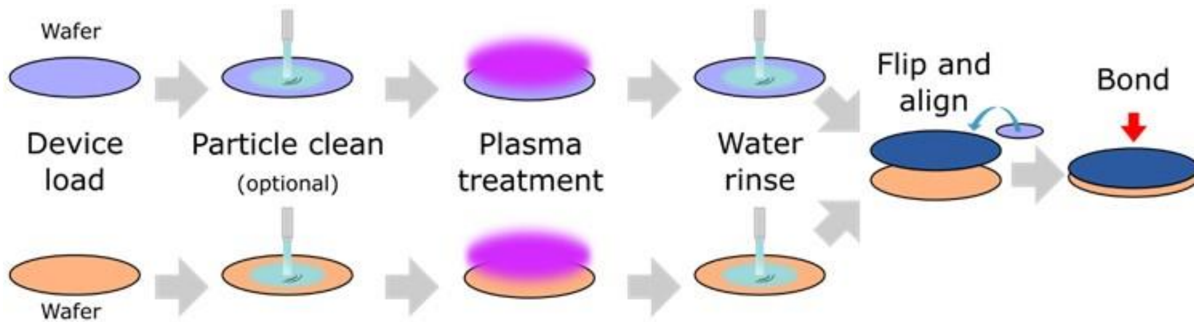

Figure 12: Schematic of the Wafer-to-Wafer Hybrid Bonding Process

Note: Two wafers are loaded into the bonding tool. Both wafers undergo a plasma treatment to activate the dielectric. One wafer is flipped without touching the front side. All dies are collectively bonded in a single bonding step.

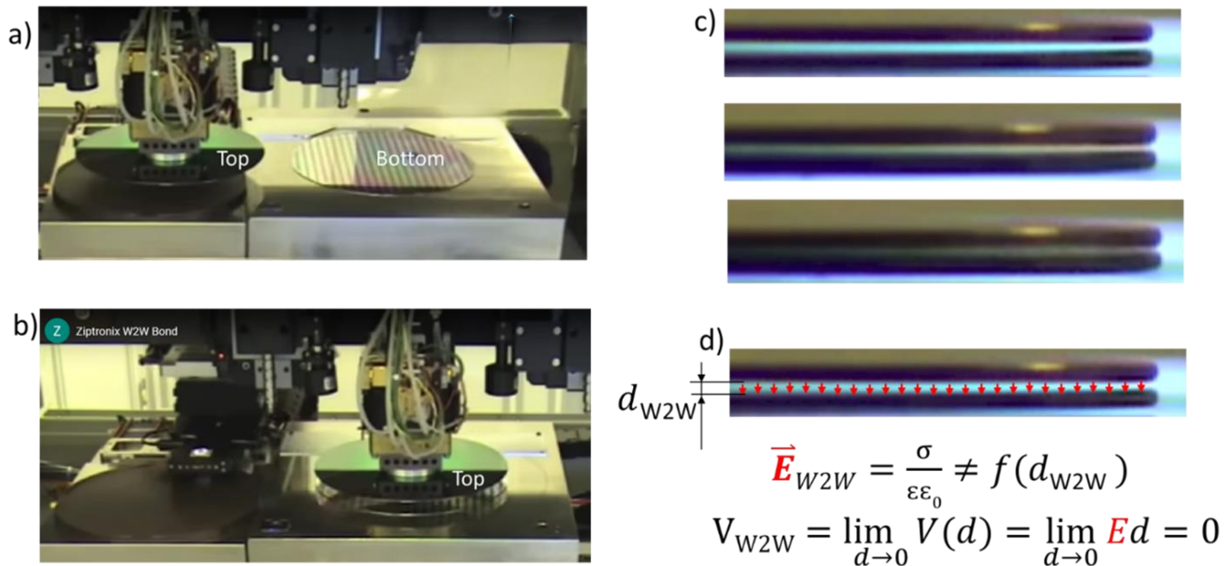

Figure 13: Wafer-to-Wafer (W2W) Hybrid Bonding

Note: a) Both top and bottom wafers are separated, ESD control is a must (top right corner), b) the top wafer gets positioned above the bottom wafer; c) gap closing between the top and bottom wafers; d) E-field between the wafers is constant (refer to Section 3.3.7) and does not depend on the distance between the wafers, the voltage between the top and bottom wafers tends to zero when the gap "d" tends to zero.

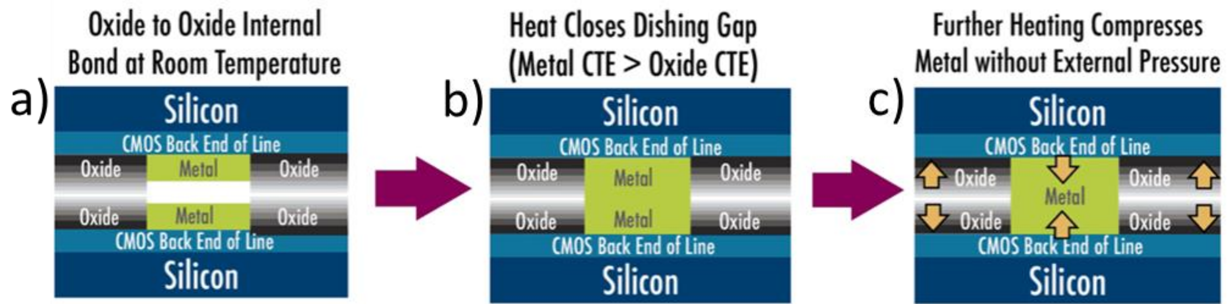

Figure 14: Illustration of W2W Hybrid Bonding

Note: a) Oxide surfaces bond wafers, while Cu vias are weakly coupled because of chemical mechanical polish dishing; opposite charges on top and bottom wafers get equalized by diffusion-tunneling across an air gap of millions of metal contacts. b, c) heating steps form an electrical contact between metals.

3.3.5 Handling of Bonded Chips

After die-to-wafer or wafer-to-wafer bonding, ESD risks are the same as for any other back-end-of-line die or wafer processing and handling step. The ESD-sensitive D2D interface is no longer exposed, except if the samples need to go to another round of 2.5D/3D bonding.

3.3.6 Testing

Another ESD exposure risk can happen during functional testing of D2D interfaces. This will be very limited due to the sheer number of D2D interfaces and the tight pitch. The subset of D2D interfaces that are targeted for testing should be treated separately and might require increased ESD protection design compared to non-tested D2D interfaces. Common rules/practices, as described in ANSI/ESD S20.20 (and similar), should be followed for grounding the test probes and the wafer, as well as the discharging of the wafer after wafer movement.

3.3.7 Voltage Suppression Effect

As two wafers come closer to each other, the capacitance between them will increase and therefore the voltage will be reduced. This is described as the voltage suppression effect.

This effect is beneficial to both die-to-wafer and wafer-to-wafer bonding processes because it reduces the risk of CDM ESD. For the sake of simplicity, we assume the charges at both bonding targets are fixed.

The following equation explains the voltage suppression effect using the parallel plate capacitor analogy.

$$C = \epsilon_0 \epsilon_r \frac{A}{d} = \frac{Q}{V} \Rightarrow V = \frac{d \cdot Q}{\epsilon_0 \epsilon_r \cdot A}$$

The parallel plate capacitor size *C* is specified as the ratio of the plate area *A* and the distance between them *d*, multiplied by the electric permittivity of free scape $\varepsilon_0 \approx 8.854$ pF/m and the relative permittivity ε_r, which for air is $\varepsilon_{air} = 1$. The same capacitor can be defined as the ratio of the charge *Q* it holds and the voltage *V* between its two plates. From these two equations follows that the voltage *V* and distance between the plates *d* are proportional.

The fact that wafers and dies in 2.5D and 3D bonding must be almost parallel to each other further helps to strengthen the voltage suppression effect and the parallel plate analogy.

A more accurate explanation of the voltage suppression effect that is directly applicable to die-to-wafer and wafer-to-wafer bonding, can be found in [Ibe2019].

3.4 Assessment of Real-World Discharges

Electrostatic charges on an integrated circuit (IC) die is either due to electrostatic induction or contact and separation of two materials, also called triboelectric charge generation. Electrostatic induction charging is similar to the charge induced on an FICDM tester. Triboelectric charging is similar to the charging that occurs when an IC is sliding down a packing tube. It is important to note that for electrostatic induction the total charge on a die is zero even though the die is at an elevated potential, while for triboelectric charging the total charge on a die is always non-zero. During assembly, a die is picked up from the dicing tape, transferred, and placed to a destination by a fully automatic robotic assembler. This movement and transfer of a die may happen multiple times before it is finally placed on another die/wafer/interposer/package. For all practical purposes, there is no manual pick-and-place die assembly steps that may result in human touching of D2D I/O interfaces. Therefore, the human body model should not be a qualification parameter.

It is required to assess the voltage generated by a die using a static voltmeter with a high spot resolution (the smallest measurement area that the meter can resolve). As described in ANSI/ESD S20.20 and ANSI/ESD SP17.1, the spot resolution of a field meter is not appropriate for the measurement of a die and will never measure the correct charging voltage on the die. This is one of many things that need to be considered when completing a process assessment on the ESD risks for D2D interfaces in a manufacturing environment. As discussed in Section 3.2, there is no standard available that describes the requirement for ESD protective measures needed in a production line for products with the low CDM robustness of D2D interfaces. The reason for this is that every description in a standard would just be valid for one specific process step with one specific tool and there are too many different tools in Industry to be covered. Even if the tool is of the same type, there might be differences in materials used or the process itself that could influence the charging or discharging risk. Therefore, the measurement techniques/methods as described in ANSI/ESD SP17.1 must be understood and applied to the tools and materials needed in D2D manufacturing to complete a thorough ESD process assessment. Many of the limits on materials as defined in ANSI/ESD S20.20 may still apply, but it is only with the measurement techniques/methods as per ANSI/ESD SP17.1, and engineering judgment, that ESD risks can be mitigated.

Chapter 4: Target Recommendations for Die-to-Die Interfaces

Harald Gossner, Intel Corporation

4.1 Introduction

The purpose of this chapter is to provide guidance for industry target levels that accounts for design constraints as well as the capability of the manufacturing process to safely limit the level of discharge in the relevant process steps for heterogeneous integration. It is acknowledged that manufacturing technology has not yet widely adjusted to the very low CDM robustness of D2D interfaces in a heterogeneous integration process flow. On the other hand, not all products using heterogeneous integration require an extremely high number of D2D interconnects. This relaxes the constraints for ESD design. These aspects are reflected in the responses to the survey, where the CDM target values vary from 3 V to > 70 V. Therefore, a roadmap to minimum target levels is provided which helps to support highly constrained designs for volume production in 2024 and beyond. These will only be manufacturable in sites that have gone through a rigorous assessment of the process to minimize ESD discharge to the lowest level. Designs that are less constrained are encouraged to design in more ESD robustness to allow more flexibility in the choice of manufacturing.

4.2 Handling of Variants of Heterogeneous Integration

The fundamental difference in the heterogeneous integration process of ESD relevance are 1) wafer-on-wafer vs. chip-on-wafer and 2) high-density 3D stacking versus 2.5D integration. A WoW process has a particular feature that during the bonding process typically the die in the center of the wafer receives the first contact (and possibly first discharge).

4.3 Targets and Roadmap

The targets are specified depending on the assembly process.

1) WoW process:
   The WoW process poses fewer ESD risks due to the small number of steps necessary to bond the two wafers together. Therefore, D2D interfaces exposed to a WoW process may not require additional ESD protection if a proper process assessment as per ANSI/ESD SP17.1 confirms that there is no risk of an ESD discharge during the processing of the wafers (see Section 3.3.4).

2) CoW process:
   D2D interfaces exposed to a CoW process require additional ESD protection. In general, a minimum CDM protection of 30 V is recommended which is compliant with the voltage balancing capability of correctly installed ionizers. In the future, a lower CDM target value is required to satisfy the design needs of area and power for a high number of D2D interconnects in the thousands to millions per die. As shown in Figure 15, it is

recommended to prepare 2.5D and 3D assembly for a target level of 3 V in a period of 5 years. It is suggested to target an intermediate step of a 5 V CDM robustness for products ramping high volume production in 2024. These products can only be manufactured in a qualified manufacturing environment with tight ESD control. The transition to a 5 V CDM target is required to support high-density D2D IO with a bond pitch of 10 µm bond pitch or less (see Figure 16). In White Paper 2 Part I (JEP157A) an intermediate CDM target of 10 V was recommended for a period between 2021 and 2024. This higher CDM target is intended to offer margin, but it is believed that a 5 V CDM target will be necessary to support D2D interfaces in the higher density bond pitch of 10 µm or less (see Figure 16). As a result, a 10 V target is no longer considered viable and has been removed from the roadmap from 2024 and beyond. It should also be noted that while a transition to a 5 V CDM target for high-density D2D interfaces will start in 2024, the expectation is that the transition to a 5 V CDM target will take some time and is expected to fully transition over approximately 4 years as shown in Figure 15.

D2D interfaces exposed to electrical testing need to comply with a minimum CDM robustness of 30 V. It has been reported in the industry survey [Q20] that there is risk in the transition to a 5 V CDM target in the production of D2D interfaces. As discussed in Chapter 3, in a well-controlled environment the limited number of front-end process steps in the D2D process makes it possible to enable ESD controls as is also necessary for example in magnetic head production.

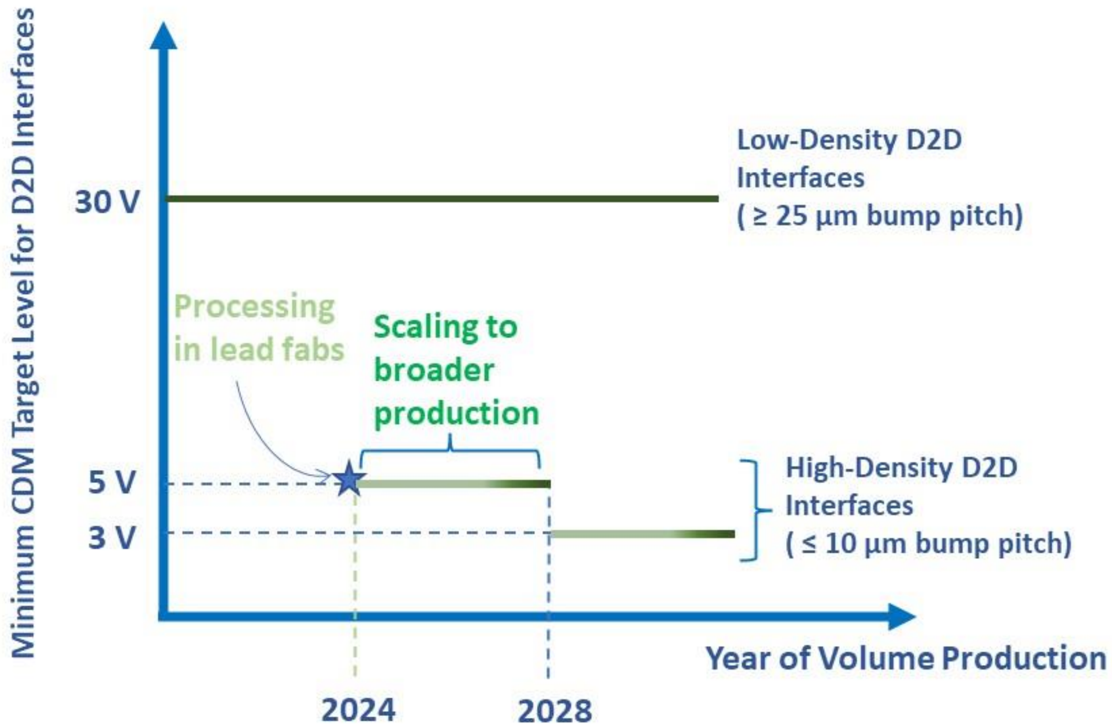

Figure 15: Roadmap of CDM Targets of Die-to-Die Interfaces

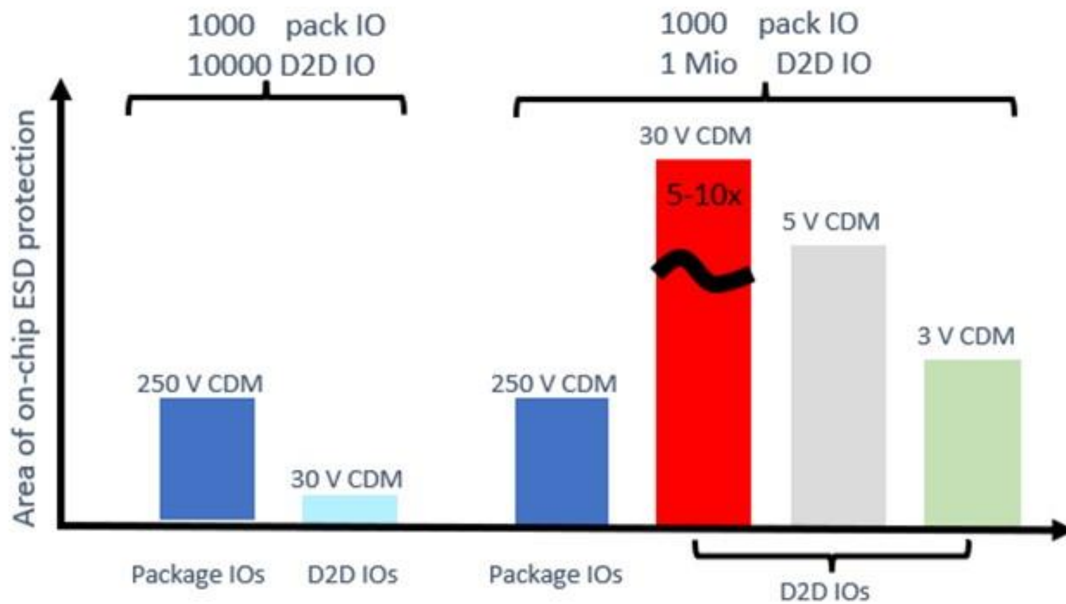

Figure 16: Area Impact of Various CDM Targets for Die-to-Die Interfaces

4.4 Conversion of V_{CDM} to Peak Current

The robustness specification of D2D interfaces in Figure 15 refers to the CDM test voltage. This needs to be correlated to a CDM peak current (i.e., I_{peak}) to guide the design of IP and to assess real-world discharge events.

An important parameter is the effective capacitance of the chiplet, which depends on the size of the chiplet. Today, the maximum die size is limited by the reticle size of about 850 mm^2. For typical chiplet sizes, the capacitance values will range between 2.5 pF to < 100 pF. Table 1 presents the peak current values for the small and large verification targets of 7.2 pF and 55 pF based on linear extrapolation from the ANSI/ESDA/JEDEC JS-002 TC125 test condition.

Table 1: Conversion Table of V_{CDM} to I_{peak} in a CDM Test Set-up According to ANSI/ESDA/JEDEC JS-002. *Note: The peak current depends on the die size. The average peak currents for the small and large calibration targets are presented.*

V_{CDM}	I_{peak} for C (die) = 7.2 pF (corresponds to a typical die area of ~ 62 mm^2)	I_{peak} for C (die) = 55 pF (corresponds to a typical die area of ~ 500 mm^2)
125 V	1.9 A	3.0 A
30 V	455 mA	720 mA
5 V	76 mA	120 mA
3 V	46 mA	72 mA

The conversion of V_{CDM} to peak current of intermediate die sizes does not follow a linear relation. However, independent of die size, the peak current depends on the parameters of the chiplet technology such as silicon substrate thickness, backside metallization, µbumps, etc.

The peak current values given in Table 1 are **worst-case values for a very low impedance discharge**. Another option for calculating peak current is discussed in Appendix C. A higher impedance in the discharge path of a typical I/O on a chiplet will reduce the peak current. For the targeted chiplet technology a more accurate voltage-to-peak current relation should be extracted based on measurements.

It has to be emphasized that the discharge generated by a CDM tester evaluating the ESD robustness of a packaged system is fundamentally different from both the discharge of a chiplet at these low voltages in a CDM tester and the real-world discharge during the 3D assembly process. The very low voltage CDM discharge is governed by a metal contact discharge. The spark impedance will not play a role here. For an ideal metal-metal contact only the impedance of the pogo pin and the 1 Ω disc resistor limit the current. However, a non-ideal metal contact can cause a larger change in the measured peak current. In the situation of a real-world discharge of a die-to-die or die-to-wafer discharge the impedance of the pogo pin does not exist. This can lead to an even higher peak current at a given voltage difference. At the same time, the voltage difference between the chiplet of a discharge drops significantly in a constant charge condition when bringing them very close together before the discharge happens. This leads to a reduction of the peak current.

Fundamentally, the CDM voltage robustness cannot be put in direct relation to a charging voltage observed in the field but must be considered as a relative degree of robustness to other components.

The waveforms of CDM-type discharges of a bare die are discussed in Appendix D. The pulse width is typically < 300 ps and the risetime can be < 100 ps. The actual real-world discharge will even be faster due to the reduced inductance without a pogo pin. Due to the low currents, the di/dt does not differ much from typical CDM discharges to packaged systems. This reduces the risk of damage due to voltages across internal inductances. However, due to the large current density in the minimally designed diode, a larger voltage overshoot can appear due to the forward recovery effect of the diodes. This is mitigated by parasitic capacitance which can help to sink the smaller discharge currents more effectively than for CDM discharges in the ampere regime. In essence, there are several counteracting factors to be considered which require further investigation.

Chapter 5: Recommendations for ESD Stress Testing of Die-to-Die Interfaces

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James Karp, AMD
Mark Styduhar, Marvell

5.1 Constraints

Considering that 2D, 2.5D, and 3D manufacturing are fully automated processes, there is no need for an HBM evaluation. For the ESD assessment of D2D interfaces CDM-type (< 1 ns pulses) testing suffices.

However, regular CDM testing (according to the ANSI/ESDA/JEDEC JS-002 standard) is generally not feasible for three reasons:

1) Small pitch µbumps that can't be accessed by the FICDM tester probe.
2) Reproducibility problems due to the large spread in FICDM peak current at low voltage.
3) A significantly large number of D2D interfaces – potentially in the hundreds of thousands per SoC.

Suitable alternative techniques, which can produce repeatable CDM-like waveforms at low-stress levels, are VF-TLP, cc-TLP, and LICCDM. Probing access to µbumps is possible for a relatively small µbump pitch (> ~25 µm). Today these three alternative stress methods are primarily ESD characterization tools due to the lack of qualification standards for the methods. All three methods are supported by test method documents. VF-TLP is supported by the standard test method (STM) ANSI/ESD STM5.5.1. As an STM, the method has been demonstrated to produce repeatable and reproducible measurement results.

LICCDM and cc-TLP are both specified in standard practice (SP) documents. SP documents describe a "best practice" to produce a measurement result but have not yet been demonstrated to produce repeatable and reproducible results. Test engineers familiar with these test methods have found no reason why these two methods could not be elevated to an STM level or the level of a qualification standard with proper supporting measurements. The question is which of these methods provides the best path to a qualification standard for CDM at very low voltages.

VF-TLP is fundamentally different from cc-TLP and LICCDM since VF-TLP is a two-pin test that creates a well-defined current path. As such VF-TLP may remain a valuable characterization tool but not be a good tool for a qualification standard. The current paths for cc-TLP and LICCDM are similar to the current path for FICDM with current flowing through the device from a single stressed pin to a distributed capacitance and are therefore better candidates for charged device qualification standards.

Three tasks need to be accomplished to have a qualification standard for the lowest voltage levels. The first is to produce supporting data for cc-TLP and/or LICCDM to show that they produce repeatable and reproducible measurements allowing them to be elevated to an STM or standards

document level. The second is to demonstrate that cc-TLP and/or LICCDM produce the same type of failures as FICDM. This is the job of the joint JEDEC/ESDA CDM Working Group. The third is to create the link between a measured current pulse and a CDM voltage.

Failure criteria will typically be based on leakage and Iddq increases since often no functional testing will be possible, as discussed in Section 5.4. Another constraint, related to the very large number of D2D interfaces, is that representative testing is required, an exhaustive test of a high number of µbumps is practically impossible.

The following devices can be considered for the ESD evaluation:

- Chiplets of the SoC
- IP macro (test chip)

In Section 5.2 the pros and cons of these options are discussed.

5.2 Device Test Options for ESD Testing of D2D Interfaces

The ESD evaluation of D2D interfaces can be considered to test chiplets, IP macros, or SoC (product). As argued in Section 5.1, standard FICDM testing is not suitable, so one of the alternative test methods; VF-TLP, cc-TLP, or LICCDM should be used.

Regardless of the device type that is ESD tested, in all cases, the primary parameter of interest is the peak current I_{peak} at failure with other parameters such as rise time playing a secondary role. Leakage and Iddq increase are used as failure criteria.

Alternatively, a target ('qualification') peak current could be set, and afterward, a functional test could be done besides the leakage and Iddq tests to enhance the test coverage.

5.2.1 ESD Testing on a Full Chiplet of the SoC

The original chiplet is used for ESD evaluation of the D2D IP. To enable direct access to the µbumps for testing per the above test methods, a moderate pitch (> ~25 µm) is required.

Advantages of testing full chiplets:

- No extra device design is needed, so a relatively cheap and convenient solution.
- Accurately resembling the situation on the final product, since the IP is qualified in the same configuration, including connections, power clamp distribution, etc.
- Takes away the need for D2D ESD testing at the SoC level using a debug package.

Disadvantage: For very tight µbump pitch (< ~10 µm) or hybrid bonding, probe access is not possible or extremely difficult and the chiplet can't be used as a test device directly.

5.2.2 ESD Testing on IP Macros

A dedicated test chip with the IP macros is used for ESD testing. This is an expensive solution but might become feasible when the IP test chip is already scheduled, e.g., for functional verification of the IP. Some provisions are needed to enable ESD testing:

- Connect selected μbumps (if too small to probe) to large, easily accessible test pads.
- The test chip should provide access to all IP test structures and include a power clamp in worst-case configuration.
- Should allow powering of the IP to enable accurate tri-state leakage testing.

Advantages of testing IP macros:

- The pad pitch can be chosen independently from the original pitch of the D2D interface.
- Full freedom to configure the D2D I/Os and power clamps in a way that allows optimal ESD characterization of the circuitry.
- Takes away the need for D2D ESD testing at the SoC level using a debug package.

Disadvantage: The configuration of the D2D I/Os, power clamp distribution, and connections differ from the SoC implementation of the interface, which means that a mismatch might exist between the results on the test chip and the SoC. It also requires thorough checking of the integration of the IP on the SoC to ensure the test chip implementation is indeed the worst case when compared to the final solution on the SoC.

5.2.3 ESD Implementation Correct by Design

Given the complexity of ESD verification on silicon, ideally, the ESD design flow should replace the need for post-silicon verification. Dedicated ESD guidelines (target level dependent) for D2D need to be provided and followed in the design phase. Pre-silicon verification tools and methodology are required to ensure the correct implementation of the ESD guidelines. The relatively low CDM targets for D2D can be exploited to simplify ESD design rules, e.g., at a low CDM level, the power domain decoupling capacitance could act as an effective clamp. In that case, a safe ESD level could be ensured by some basic checks like a primary diode size and a minimum level of metal-insulator-metal (MIM) capacitance, see Section 6.2 for more details.

5.3 Recommended ESD Evaluation Flow

In past sections, test methods and test device type options for the ESD evaluation are discussed with pros and cons. The recommendation is a flow based on **ESD evaluation on the IP test macro** (Section 5.2.2). The major benefits are:

- An IP test chip is often planned anyway to validate the functional performance of the IP.
- It is relatively simple to add some dedicated bumps to enable direct access to instances of all D2D I/O types for the ESD analysis.
- With minimum ESD performance confirmed on the IP test chip, no further ESD analysis of the D2D circuitry on the SoC is needed anymore.
- Some basic checks at the SoC level to ensure correct integration of the D2D IP will suffice.

This is complemented by a **correct-by-design methodology** (Section 5.2.3), which is especially appropriate in case of very low CDM target requirements. Verification tools are used to check the correct implementation with respect to the (at low CDM targets, typically basic) guidelines.

The combination of ESD evaluation at the IP test chip level with correct-by-design methodology takes away the need for silicon evaluation of the D2D interfaces on the SoC level.

5.4 Post-Stress Validation

It is important to note that, unlike packaged product CDM qualification, D2D I/O post-stress validation can be limited to the immediate D2D I/O circuitry. The reason for this simplification is that the CDM I_{peak} for D2D I/O is more than an order of magnitude lower than the CDM I_{peak} of packaged dies. The small CDM peak current cannot inflict damages at internal nodes observed at CDM qualification of packaged dies [Kar2016B], [Kar2008]. That said, for evaluation of the CDM strength of D2D I/O, it is sufficient to compare the I-V curves “before” and “after” CDM test.

Chapter 6: Pre-silicon Verification Challenges and Approaches

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Nicolas Richaud, Intel Corporation
JY Song, Samsung

6.1 Introduction

Chapter 6 describes the pre-silicon verification challenges and possible approaches for D2D interface designs. ESD threats for D2D interfaces occur during the automated D2D assembly process, which means that only CDM verification needs to be considered.

Various verification methodologies have been employed to verify the CDM robustness of traditional ESD protection designs [Q07], from simple resistance network analysis to modern dynamic high-current ESD simulation tools. Most of the traditional verification methodologies can also be applied to D2D interface designs with reduced ESD targets as mentioned in Chapter 4. However, there are important differences between the traditional ESD protection network and those of D2D interfaces, which introduce additional advantages and challenges: A small peak current level and an extremely large number of exposed signal bumps. The small peak current requirement can lead to a smaller area footprint and thus a more flexible placement of ESD protections. In case the driver size is sufficiently large, the driver junction diodes might be sufficient to replace the main ESD protection diodes partially or fully. Checking an extremely large number of µbumps requires proportionally heavy computational power, which might become a practical problem for the verification tool.

6.2 Verification Methodology

A set of reusable verification methodologies is listed below. Availability of CDM (VF-TLP) characteristics of both the ESD devices and victim devices is necessary.

- Topology check:
  - Similar to the non-D2D ESD protection network, the topology (configuration of protection diodes, power clamps, victims) must be checked. The D2D bumps can be considered as signal bumps, for which well-established connection rules are available. In addition to the usual topology check rules, the minimum driver size can be checked for self-protection design.
  - In D2D designs the same IPs/blocks are expected to be used repeatedly. The topology of the IPs/blocks should be fully checked. At the full chip level, hierarchical verification of topology checks based on abstract information from IPs/blocks can be applied in case the electronic design automation (EDA) tools support the functionality.

- ESD resistance network analysis:
  - The wire resistances (causing IR drop), ESD device on-resistance, and on-voltage of the D2D interface protection can be calculated by a simple formula to check the clamping level compared with the victim breakdown level. The "low" CDM target

creates a larger tolerance for resistivity from µbump to ESD protection or between ESD protection (like from diode to clamp). However, it is interesting to note that the reduced size of the ESD protection element also creates a larger resistivity path to connect to it. The point-2-point (p2p) analysis tool should not only check the power delivery network but also the paths from µbumps through the primary protection diodes.

- Current density check:
  - The same current density rule as for the non-D2D design can be applied to the D2D interfaces. Full current density analysis is supported by various EDA tools. Given the large number of bumps, current density verification on the power grid can be a challenge for the EDA tools. The current density analysis tool should cover the paths through the primary protection diodes for CDM discharge current events.

- High-current dynamic CDM simulations:
  - If the CDM behavior of ESD devices is included in the device models, a dynamic CDM simulation can provide accurate victim voltage and current levels. The result of a dynamic simulation heavily depends on the accuracy of the small-sized ESD device model and the victim breakdown voltage. The dynamic simulation is computationally expensive and may not be practical without netlist simplification.

To protect the D2D interface from ESD stress different design strategies can be employed. Power-clamp-based protection is a well-known protection methodology, to which most of the above-described methodologies are relatively easily applicable. Capacitance-based protection can be another option to protect the D2D I/O due to the small peak current level. Details of the two protection strategies are discussed below.

6.2.1 Clamp-Based Protection

To protect the power rails from an ESD event a common approach is to use a power clamp consisting of a large transistor ('BigFET') that shorts power and ground during the ESD event. The transistor is controlled by an RC circuit that triggers the transistor during an ESD transient discharge [Section 4.5 ESD TR18.0-01-14 of ESDA WG18] as shown in Figure 17.

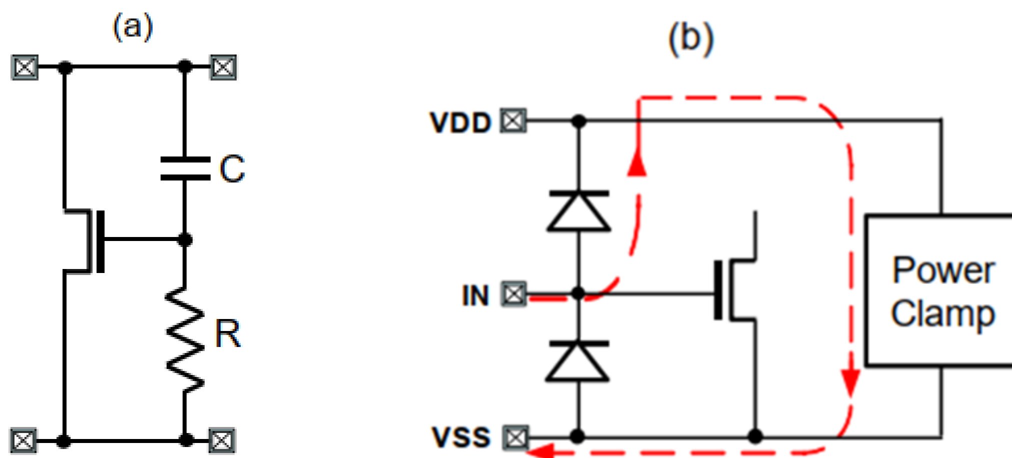


Figure 17: (a) Power Clamp with Simple RC Circuit (b) Rail Clamp Protection Path

This protection approach can be applied to the D2D interface. The area footprint of the transistor inside the clamp can be reduced based on the lower CDM target of the D2D interface. A further, significant area saving can be achieved by considering that the RC time constant can be reduced to cover CDM events only (no need for HBM).

The resistance path to the ESD power clamp is an important parameter to control, especially the resistance from the upper diode of the first stage protection to the power clamp. Tools and flow methods like static point-to-point resistor checks already exist and could be reused to verify the resistance value between two ESD elements or back-annotated resistance path for the ESD transient simulation.

The reduced target for ESD will allow a larger resistance value between ESD elements, which could impact the compute resource needed to run the verification. Key challenges are the parasitic extraction of the power grid as the length of the path to extract could be longer, and the high number of interfaces to check when a small bump pitch is used.

6.2.2 Capacitor-Based Protection

An alternative approach could be to rely on a capacitor instead of a transient clamp, as shown in Figure 18. Modern, high-speed D2D interfaces require a stable power supply and normally large decoupling capacitance in the range of nano Farads. These capacitors could be utilized as power clamps and replace explicit clamp-based power protection.

While reducing the ESD area footprint could be attractive for the designer, it brings new challenges for verification.

Tools and flow methods may need to be enhanced to evaluate the effective capacitance value between the power rail and ground, considering the different types of capacitors (MIM, metal-oxide-metal, and metal-oxide-semiconductor) and the distributed character of the capacitors with respect to each D2D interface circuit.

Back annotation of capacitor values for an ESD transient simulation in a large network could be another challenge, especially for a distributed capacitor like a MIM capacitor.

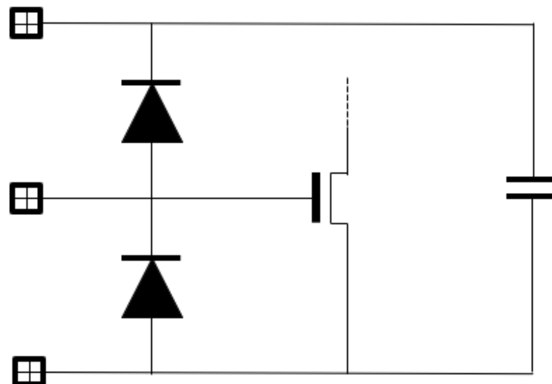


Figure 18: Capacitor Used to Protect the Power Rail Instead of an ESD Power Clamp

Chapter 7: Roles and Responsibilities in the Value Chain

Harald Gossner, Intel Corporation
Charvaka Duvvury, iT2 Technologies
James Karp, AMD

7.1 Introduction

Many players need to be involved to guarantee the safe manufacturing of D2D interfaces. Their responsibilities are varied to maintain the value chain. Nevertheless, protection design targets and manufacturing capabilities need to be well aligned to guarantee safe production. Some of these are outlined in this chapter. However, the outcome depends upon how well these are coordinated and synchronized. In a nutshell, while different entities in the product definition, design, manufacture, and test have primary responsibilities, there needs to be considerable communication between the entities to ensure a successful product.

7.2 Semiconductor Fab

7.2.1 Roles

Defines the 2D, 2.5D, and 3D integration options.

7.2.2 Responsibilities

- Manufactures functional integrated circuits consistent with the definition of the technology and the defined packaging options.
- Development and implementation of advanced ESD protection structures consistent with the definition of the technology and the defined packaging options.
- Automated test equipment (ATE) capabilities and failure analysis (FA) resources.
- Develop process design kit (PDK) and assembly design kit (ADK) for use by design enablement.

7.3 OSAT Packaging & Assembly

7.3.1 Roles

Heterogeneous integration process assessment and optimization of 2D, 2.5D, and 3D assembly and test.

7.3.2 Responsibilities

- Implementation of advanced ESD protection consistent with the definition of the technology and the defined packaging options.
- ATE capabilities and FA resources.
- Define the level of ESD control the OSAT is capable of with current equipment and controls for use by the IP development team.

7.4 Design Enablement

7.4.1 Roles

Installs the PDK/ADK from the FAB for use by the IP development team.

7.4.2 Responsibilities

- Provide technical support to the IP developer in the use of the PDK tools used to design and verify ESD and latch-up solutions.

7.5 IP Developer

Includes both internally developed IP and 3rd party IP.

7.5.1 Roles

Defines the ESD and latch-up requirements for the IP being developed.

7.5.2 Responsibilities

- Develop viable ESD and latch-up solutions for inclusion in the IP.
- Design ESD and latch-up solutions that allow the circuit to meet its power, performance, and area requirements.
- Design IP that passes ESD and latch-up lab testing.

7.6 Fabless Semiconductor Company or Integrated Device Manufacturer

7.6.1 Roles

- Defines the ESD and latch-up requirements.
- Performs ESD & latch-up lab testing of the IP/chiplets/SoC.

7.6.2 Responsibilities

- Assure IP, chiplet, or SoC passes ESD and latch-up testing requirements.

Appendix A: Questions of the Industry Survey

Type of questions:

single choice ○

multiple choice ☐

text based

1. [Q01] Which company do you represent?

2. [Q02] In which country are you working?

3. [Q03] What type of business is your company?

- ☐ IP vendor
- ☐ SOC design
- ☐ Foundry
- ☐ OSAT
- ☐ N/A
- ☐ Other

4. [Q04] Do you apply lower CDM targets for d2d interfaces compared to external balls?

- ○ Yes
- ○ No
- ○ N/A

5. [Q05] Do you apply different CDM target levels for d2d interfaces depending on the type of 2.5D or 3D process?

- ◯ Yes
- ◯ No
- ◯ N/A

6. [Q06] Do you verify lower CDM targets for d2d in presilicon verification (on schematics and/or layout level)?

- ◯ Yes
- ◯ No
- ◯ N/A

7. [Q07] How do you verify lower CDM targets for d2d in presilicon verification?

8. [Q08] Is there a need to lower the targets for d2d for your future products to satisfy PPA (Power, Performance, Area) constraints?

- ◯ Yes
- ◯ No
- ◯ N/A

9. [Q09] To your opinion, is there a need to align on industry standard CDM target levels for d2d interfaces?

- ◯ Yes
- ◯ No
- ◯ N/A

10. [Q10] To your opinion, is there a need to define ESD control standards for d2d processes?

- ◯ Yes
- ◯ No
- ◯ N/A

11. [Q11] Are you defining the CDM target for d2d interfaces in ...

- ◯ CDM voltage
- ◯ Peak current
- ◯ Both
- ◯ N/A

12. [Q12] (if possible to share) what are the minimum CDM current target levels for d2d interfaces?

- ◯ > 10 mA
- ◯ > 50 mA
- ◯ > 100 mA
- ◯ > 300 mA
- ◯ N/A
- ◯ Other

13. [Q13] (if possible to share) what are the minimum CDM voltage target levels for d2d interfaces?

- ◯ > 3 V
- ◯ > 5 V
- ◯ > 10 V
- ◯ > 30 V
- ◯ > 70 V
- ◯ N/A
- ◯ Other

14. [Q14] What kind of protection structure for d2d ESD CDM solution is used?

- ☐ Diodes
- ☐ Local clamps
- ☐ Self-protection
- ☐ N/A

15. [Q15] Do you have dedicated ESD guidelines for d2d?

- ☐ No
- ☐ Different device (diode, IO transistor) size
- ☐ Power clamps
- ☐ N/A

16. [Q16] What is the critical point in time when products with lower CDM targets for d2d interfaces start volume production?

- ◯ 2022
- ◯ 2024
- ◯ Beyond 2026
- ◯ No plan
- ◯ N/A

17. [Q17] Do have experience with d2d fails?

- ◯ Yes
- ◯ No
- ◯ N/A

18. [Q18] How were the fails detected?

- ☐ Wafer level test
- ☐ ATE test (functional test)
- ☐ Customer
- ☐ N/A
- ☐ Other

19. [Q19] Where have the fails occurred in the process?

- ☐ Testing (e.g. wafer level)
- ☐ Die attach
- ☐ Not known
- ☐ N/A
- ☐ Other

20. [Q20] From a manufacturing perspective, what is considered as minimum safe voltage level?

- ◯ > 3 V
- ◯ > 5 V
- ◯ > 10 V
- ◯ > 30 V
- ◯ > 70 V
- ◯ N/A
- ◯ Other

21. [Q21] Have you run hardware experiments (with statistics) to confirm the minimum safe level?

- ◯ Yes
- ◯ No
- ◯ N/A

22. [Q22] What experiments did you do to confirm the minimum safe level?

23. [Q23] Based on your experiments, to what maximum voltage are you able to limit the charging of your wafer/dies in your production environment?

- ◯ > 3 V
- ◯ > 5 V
- ◯ > 10 V
- ◯ > 30 V
- ◯ > 70 V
- ◯ N/A
- ◯ Other

24. [Q24] Are you able to measure a discharge current of your charged wafer/die in production to determine the risk?

- ◯ Yes
- ◯ No
- ◯ N/A

25. [Q25] Would a robustness value in current (i.e. current limit) for your ESD sensitive wafer/die be useful for you?

- ◯ Yes
- ◯ No
- ◯ N/A

26. [Q26] Are you performing an ESD risk assessment in your production lines?

- Yes
- No
- N/A

27. [Q27] What document are you using to perform such an ESD risk assessment in your production lines?

28. [Q28] How often are you performing such an ESD risk assessment in your production lines?

29. [Q29] A document for ESD process assessment is ANSI/ESD SP17.1. Is SP17.1 good enough for a risk assessment for d2d assembly?

- Yes
- No
- N/A

30. [Q30] What is missing to ANSI/ESD SP17.1. Is SP17.1 to be sufficient for a risk assessment for d2d assembly??

31. If you would like to receive a copy of the final report, please provide an e-mail address to which it should be sent

Appendix B: Results of the Industry Survey

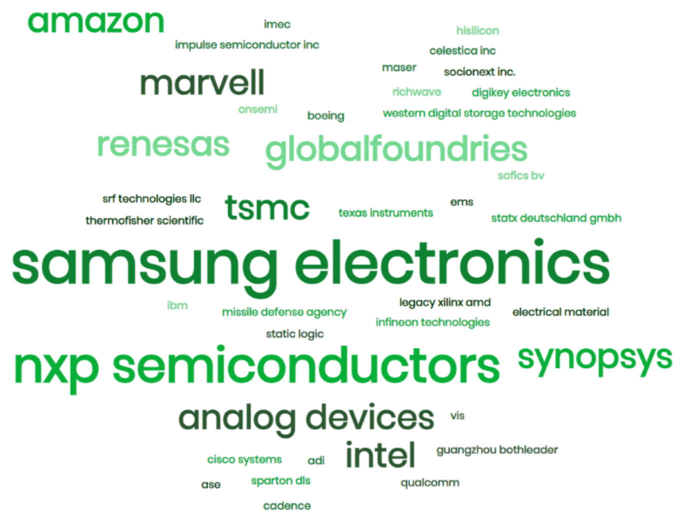
B.1 Introduction

In Appendix B the detailed results of all survey questions are presented.

B.2 Survey

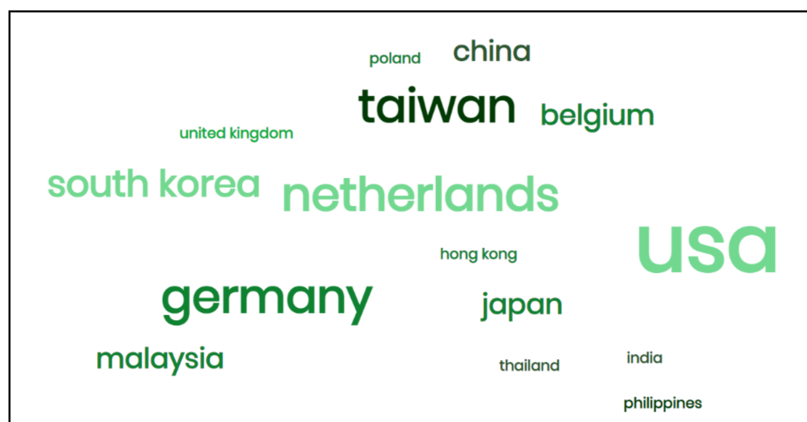
Word Cloud representation of Q1 & Q2: Font size corresponds to the frequency of the answer. Color and positioning are not conveying any information but are merely design choices.

1. [Q01] Which company do you represent?



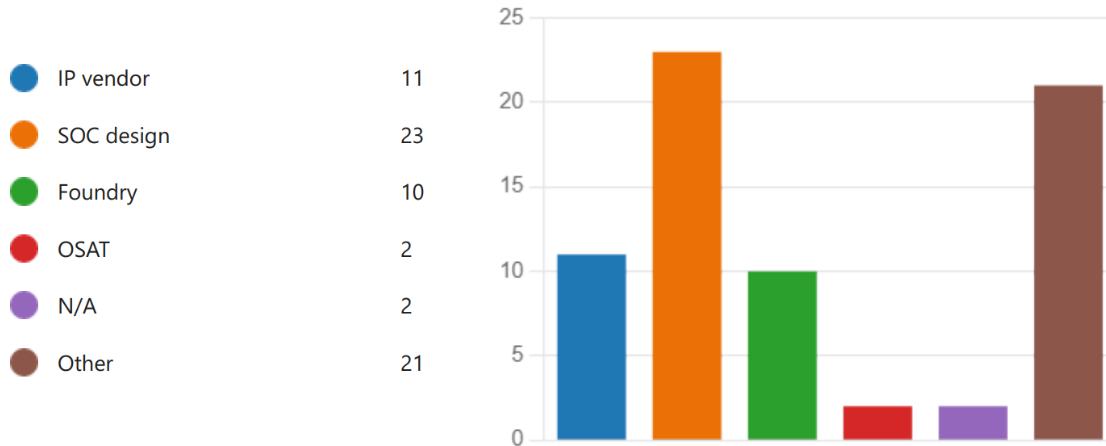
Samsung Electronics (4x), NXP Semiconductors (3x), Amazon (2x), Analog Devices (2x), GlobalFoundries (2x), Intel (2x), Renesas (2x), Synopsys (2x), TSMC (2x), Marvell (2x), ADI, ASE, Boeing, Cadence, Celestica Inc, Cisco Systems, DigiKey Electronics, EMS, MASER, Guangzhou Bothleader, HiSilicon, IBM, imec, Impulse Semiconductor Inc., Infineon Technologies, Legacy Xilinx AMD, Missile Defense Agency, onsemi, Qualcomm, Richwave Technology Corp., Socionext Inc., Sofics BV, Sparton DLS, SRF Technologies LLC, Static Logic, Stat-X Deutschland GmbH, STMicro-Electronic, Texas Instruments, Thermofisher Scientific, VIS, Western Digital Storage Technologies; self-employed (2x)

2. [Q02] In which country are you working?



United States of America (24), Germany (5x), Netherlands (5X), Taiwan (5x), Belgium (2x), China (2x), Japan (2x), Malaysia (2x), South Korea (2x), Philippines, Poland, South Korea, Thailand, United Kingdom, Hong Kong, India

3. [Q03] What type of business is your company?



Others including:

- Manufacturer [7x]
- Manufacturer, including design, component assembly, test, and next-level assembly
- Electronic distributor
- GMR/TMR device sensor for hard disk drive
- System company + IC design
- Consultant [2x]
- Aerospace
- Department of Defense
- Defense contractor
- Consumer electronics
- Insulating material
- Reliability and failure analysis lab
- Research institute

4. [Q04] Do you apply lower CDM targets for d2d interfaces compared to external balls?

5. [Q05] Do you apply different CDM target levels for d2d interfaces depending on the type of 2.5D or 3D process?

6. [Q06] Do you verify lower CDM targets for d2d in presilicon verification (on schematics and/or layout level)?

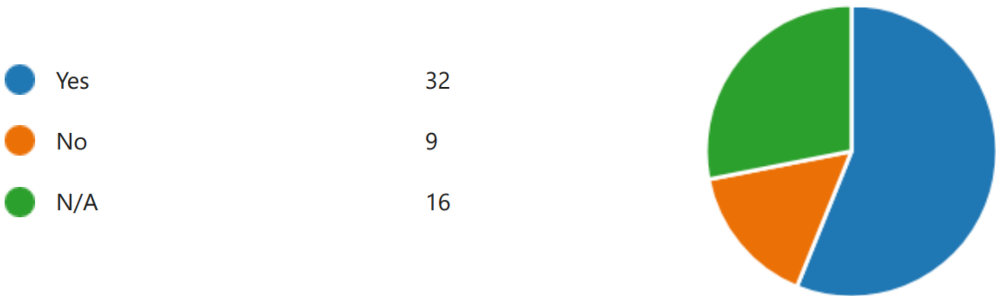
7. [Q07] How do you verify lower CDM targets for d2d in presilicon verification?

Method	Simulation	LV e.g., via PERC	Silicon data-driven	Proprietary
# of responses	7	6	2	2

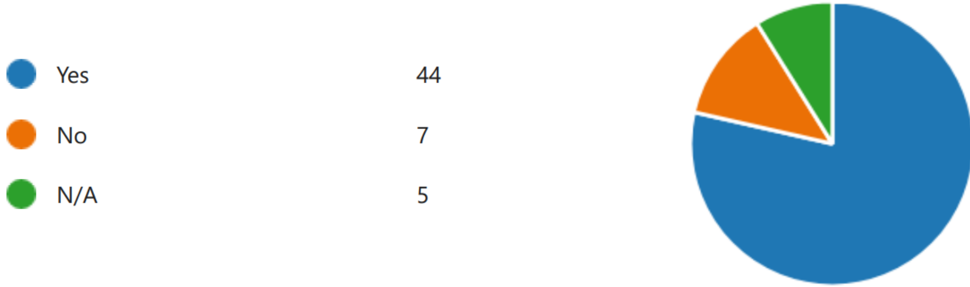
Further responses (1x mentioned):

- Technical Data Sheet
- In general: Using foundry-provided ESD design methodology.
- Correct by construction (but that may be out of date).
- By Cell Level
- Or gates to known answers and errors per each path.

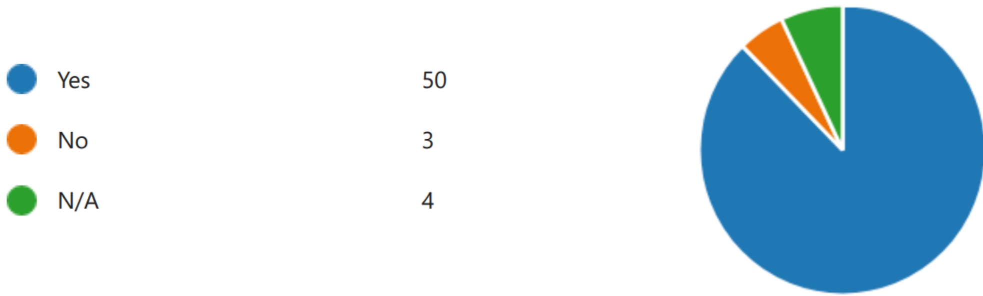
8. [Q08] Is there a need to lower the targets for d2d for your future products to satisfy PPA (Power, Performance, Area) constraints?



9. [Q09] To your opinion, is there a need to align on industry standard CDM target levels for d2d interfaces?



10. [Q10] To your opinion, is there a need to define ESD control standards for d2d processes?

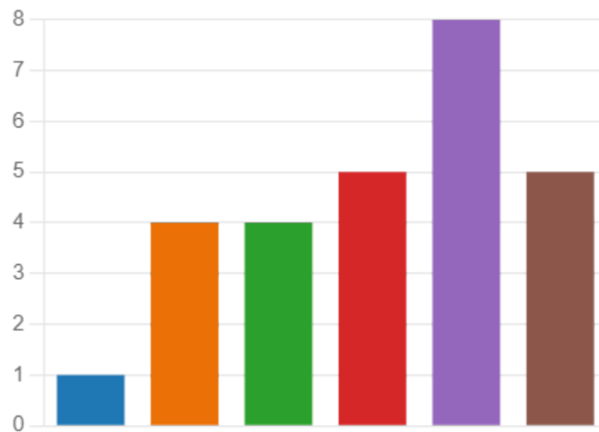


11. [Q11] Are you defining the CDM target for d2d interfaces in ...

CDM voltage	15
Peak current	9
Both	18
N/A	15

12. [Q12] (if possible to share) what are the minimum CDM current target levels for d2d interfaces?

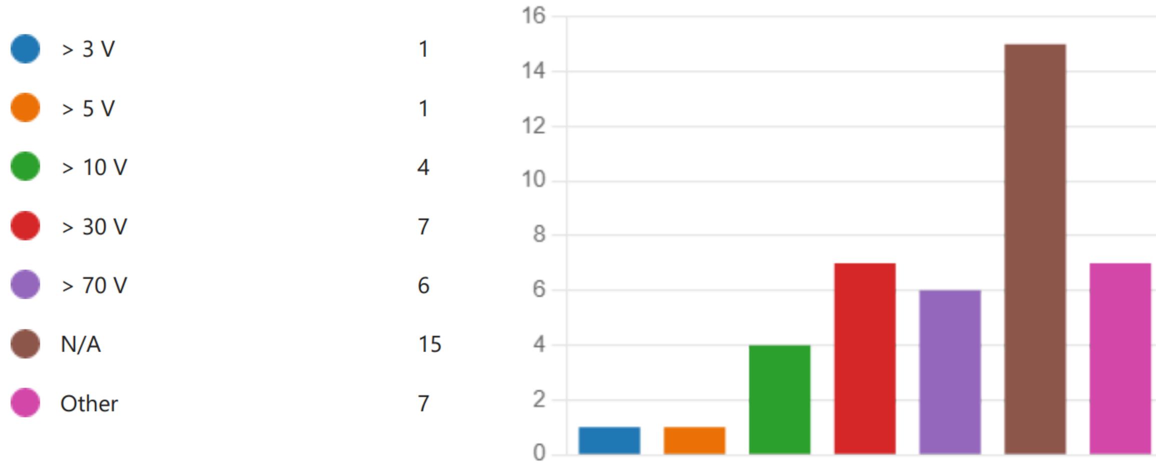
> 10 mA	1
> 50 mA	4
> 100 mA	4
> 300 mA	5
N/A	8
Other	5



Others including:

- Varying from 40 mA to 1 A depending on the interface protocol and customer request.
- Historically we have designed to 1 A. Many customer requirements are now 100-300 mA.
- TMR device connecting is limited to less than 1 mA.
- Die size dependent.
- It will depend on which D2D interfaces.

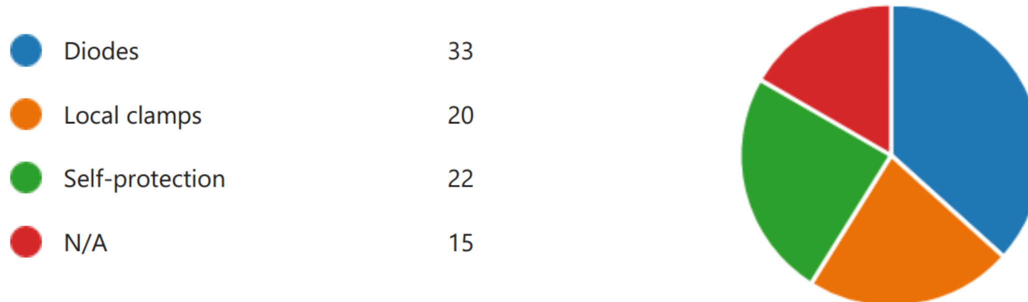
13. [Q13] (if possible to share) what are the minimum CDM voltage target levels for d2d interfaces?



Others including:

- Target > 250 V
- 30-70 V depending on the customer.
- D2D interface mode dependent, may face different manufacturers.
- 125 V

14. [Q14] What kind of protection structure for d2d ESD CDM solution is used?



15. [Q15] Do you have dedicated ESD guidelines for d2d?

No	25
Different device (diode, IO trans...	20
Power clamps	7
N/A	11

16. [Q16] What is the critical point in time when products with lower CDM targets for d2d interfaces start volume production?

2022	12
2024	11
Beyond 2026	4
No plan	7
N/A	22

17. [Q17] Do have experience with d2d fails?

Yes	10
No	32
N/A	14

18. [Q18] How were the fails detected?

Wafer level test	4
ATE test (functional test)	7
Customer	3
N/A	1
Other	1

Others including:

- At system-level testing

19. [Q19] Where have the fails occurred in the process?

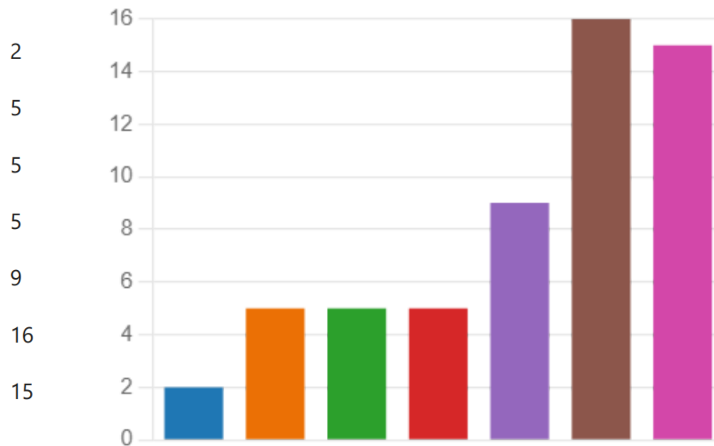
Testing (e.g. wafer level)	3
Die attach	2
Not known	5
N/A	1
Other	3

Others including:

- HBM failure, the root cause was found to be metallization weakness in the routing.
- ESD (pre) qualification.

20. [Q20] From a manufacturing perspective, what is considered as minimum safe voltage level?

> 3 V	2
> 5 V	5
> 10 V	5
> 30 V	5
> 70 V	9
N/A	16
Other	15



Others including:

- > 100 V with Class 0 controls needed.
- Depends on technology.
- Manufacturer dependent
- 125 V
- 35 V
- 50 V [2x]
- Depending on the measurement technique.
- Depends on the robustness design of the processed product.
- 200 V as said in the ANSI/ESD S20.20-2014 standard.
- Not sure (2x)

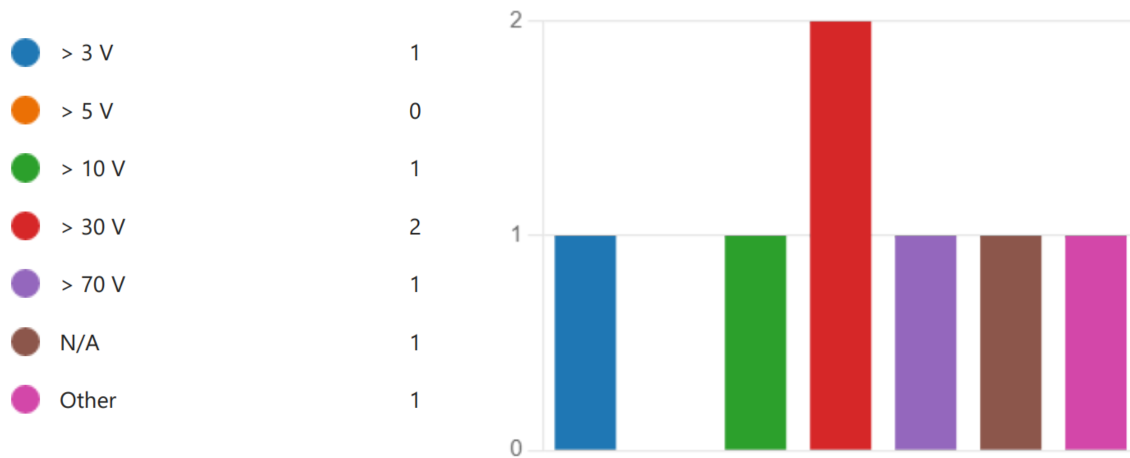
21. [Q21] Have you run hardware experiments (with statistics) to confirm the minimum safe level?

Yes	7
No	32
N/A	18

22. [Q22] What experiments did you do to confirm the minimum safe level?

- CDM tests on different protection levels.
- VF-TLP
- 1 ns VF-TLP
- Field meters / ESD detectors
- Processing dies with D2D I/Os of different protection levels.
- D2D I/O ESD diode width: none, 5u, 10u, where none: came out the best.

23. [Q23] Based on your experiments, to what maximum voltage are you able to limit the charging of your wafer/dies in your production environment?

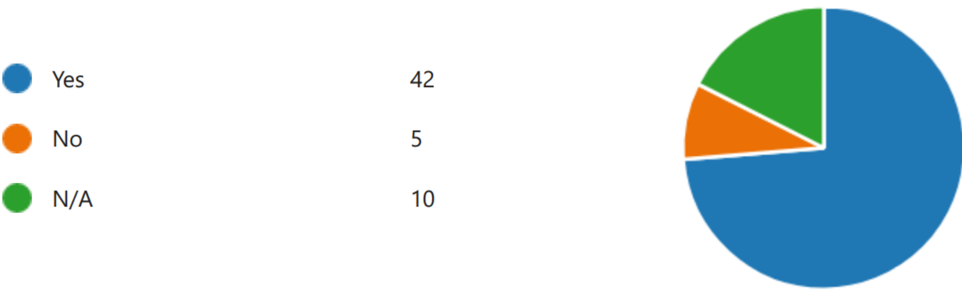


Others including:

- Production environment certified w.r.t. ANSI/ESD S20.20-2014 standard.

24. [Q24] Are you able to measure a discharge current of your charged wafer/die in production to determine the risk?

25. [Q25] Would a robustness value in current (i.e. current limit) for your ESD sensitive wafer/die be useful for you?



26. [Q26] Are you performing an ESD risk assessment in your production lines?

27. [Q27] What document are you using to perform such an ESD risk assessment in your production lines?

ESD control reference	S20.20	JESD625	IEC61340	SP17.1	Proprietary
# of responses	16	2	3	4	8

Further responses (1x mentioned):

- ESD TR53 for human/facility/environment, ANSI/ESD SP10.1 for process equipment.
- SEMI E78, SEMI E43, American Society for Testing and Materials D257-07.
- Draft standard test method, standard test method.
- ST BEMT ESD Controlled Document
- RL1013 ESD Forum
- JEDEC

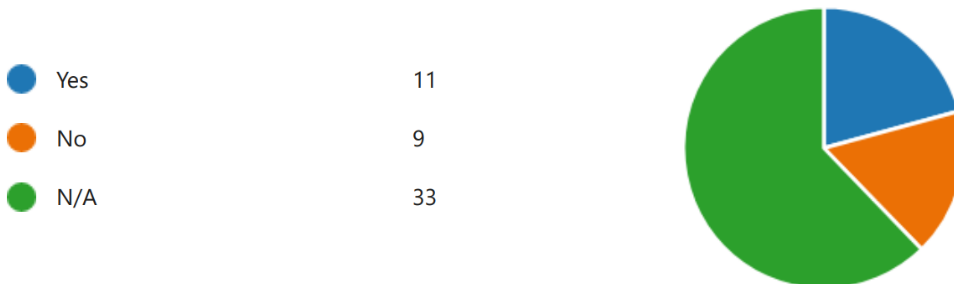
28. [Q28] How often are you performing such an ESD risk assessment in your production lines?

frequency	new product	max yearly	half-yearly	quarterly	weekly	As per S20.20
# of responses	7	4	1	4	1	2

Further responses (1x mentioned):

- Weekly, monthly, and quarterly for different items.
- Multiple times a year.
- Initial, 3 months, 6 months, and annual thereafter.
- When ESD damages our product.
- If there are any ESD-related failures.
- If a concern arises during a production run.
- When the technology or sensitivity is predicted to become more sensitive.
- Depends on the test but random samples are pulled and tested as soon as one test is finished next one is pulled for verification in a dedicated area.
- On an as-needed basis.
- Depends
- ESD risk assessments are done routinely. Checking intervals are variable depending on the items.
- Considering a process for doing this in a "radio frequency process" line.
- Do not know; N/A

29. [Q29] A document for ESD process assessment is ANSI/ESD SP17.1. Is SP17.1 good enough for a risk assessment for d2d assembly?



30. [Q30] What is missing to ANSI/ESD SP17.1. Is SP17.1 to be sufficient for a risk assessment for d2d assembly??

- How to assess the capability of safe ESD handling? Assembly follows ANSI/ESD S20.20 but there are items not addressed by current ANSI/ESD S20.20 on automated handling equipment and machine parts that directly handle the work in progress.
- ANSI/ESD SP17.1 describes mostly a procedure, there's a limited definition of corresponding specs or criteria.
- Not enough use cases to be valid. Needs a narrower focus for each area and more areas.
- ESD risks (CDM) tremendously change as the D2D device is assembled from a wafer, die, module, and assembly. ANSI/ESD SP17.1 or ANSI/ESDA/JEDEC JS-002 does not alert the reader to this challenge in D2D manufacturing processes.
- CDM current specification limit.
- More details for a D2D process assessment.
- More clarity on measuring current and capacitance (methods) in process step situations; key steps known to have issues.
- Measurement of current, and process vehicles for measuring charge / current discharge in a production line.
- N/A

Appendix C: Using Chiplet Self-capacitance to Derive Relationship Between CDM Voltage and Peak Current

James Karp, AMD

C.1 Summary

Electrostatic charges on an IC die are either due to electrostatic induction or triboelectric charge generation. Electrostatic induction charging is similar to the charge induced on an FICDM tester. Triboelectric charging is similar to the charging that occurs when an IC is sliding down a packaging tube. It is important to note that for electrostatic induction the total charge on a die is zero, but the die is at an elevated potential due to its presence in an electric field due to a nearby conductor at elevated potential or from being close to a charged insulator. For triboelectric charging, the total charge on a die is always non-zero.

During chiplet assembly, the ability of a chiplet to accumulate triboelectric charges has to be related to the self-capacitance C_s [Kar2016A]. It was shown both analytically and numerically that the capacitance of a conductor in isolation, i.e., self-capacitance C_s, is proportional to the square root of a conductor surface as follows: [Cho1983]

$$C_S = C_f \varepsilon \varepsilon_0 \sqrt{4\pi S} \quad (1),$$

where S is the surface area of the conductor and C_f is the shape factor which typically varies from 0.9 to 1.1. For example, for a field-programmable gate array (FPGA) die with L ≈ 29 mm and W ≈ 11 mm [Kar2016A], C_f = 0.931 [Cho1983]. Substituting these parameters in (1), gives self-capacitance of the FPGA die $C_s \approx 0.75$ pF. Normalized to the unit area, the self-capacitance of a 1 square mm chiplet is estimated as $C_s \approx 0.043$ pF.

The charge Q_{FPGA} on the FPGA die at voltage V_{CDM} is $Q_{FPGA} = C_s \bullet V_{charging}$. By characterizing the CDM-type discharge shape by peak current and the full width at half maximum (FWHM), the following equation can be derived:

$$I_{PEAK} \approx C_S V_{CDM} / W_{PULSE} \,[\text{mA}] \quad (2),$$

where C_s is the chiplet self-capacitance [pF], V_{CDM} is CDM voltage [V] and W_{PULSE} is the FWHM [ns], [Kar2016A].

When the calculated normalized self-capacitance value of (1) is substituted in (2), the following equation is obtained:

$$I_{\text{PEAK}} \approx 0.2 * \sqrt{A_{\text{Chiplet}}\,[mm^2] * V_{\text{charging}}\,[V]} \qquad (3),$$

where $A_{Chiplet}$ is the area of the chiplet in square mm and $W_{PULSE_}$is approximated by 0.2 ns. This equation can be used for a rough estimation of the expected peak current at a given CDM voltage as a function of the chiplet area for the handling steps of dies in a D2D assembly process.

Appendix D: EM Simulation of a Die-to-Die Discharge

Pasi Tamminen, Danfoss

D.1 Summary

There is limited information available about real-world discharge current waveforms between dies during D2D assembly. An ESD event from a die has similar initial conditions as with discharges from an IC package. Here the discharge current waveform depends on initial charges, capacitances, and discharge path. Similarly, the quasistatic ESD source capacitance depends on the size, location, and design of the die.

There are also differences between D2D discharges and ESD events in a CDM tester.

- Due to the relatively low static voltage differences between dies Paschen curve does not apply. In addition, there is a narrow µm range gap, or no gap at all, between dies at the discharge moment. In this case, the series inductance along the discharge path can be in the pH range instead of about 10 nH typically found in CDM testing.
- When a charged die contacts another conductor the contact resistance can vary from almost zero Ω to some unknown higher value. This depends on, for example, the voltage difference, contact force, temperature, surface area, surface cleanliness, surface oxidation, and roughness of surfaces. With voltage differences below 10 V the contact resistance can be tens of ohms.
- The voltage difference at the discharge moment depends on the initial static charge, charge distribution, and mutual capacitive coupling between dies just before the discharge. It can be hard to predict the discharge voltage by measuring a die potential or charge when it is picked up.
- The physical size of dies varies from a few square millimeters up to 850 mm^2, thus, ESD risks should decrease with a smaller size due to a lower source ESD capacitance. However, a smaller die can produce a faster current rise time and smaller dies can get higher initial voltages with the same amount of charge.

Due to the previous differences, D2D discharge events do not necessarily resemble typical CDM discharges due to a faster current rise time, shorter pulse length, different series resistance, and smaller total charge transfer. It is also challenging to measure fast discharge events with low initial potential and varying contact resistance. The required measurement bandwidth can be >10 GHz, and it can be difficult to measure real-world discharge current waveforms without changing the discharge scenario.

3D electromagnetic solvers can predict discharge current waveforms with varying discharge parameters. However, electromagnetic simulation tools cannot solve contact resistance values. Figures C.1 and C.2 present two example scenarios where a smaller die or IC contacts a larger component with varying die size and contact resistances.

In Figure C.1 the die is an ideal solid 0.4 mm thick square aluminum block with a 10 µm air gap to the ground plane. The potential difference is 10 V and there is 10 Ω of series resistance and 50

pH of inductance along the discharge path. The source capacitance varies from about 0.5 pF to about 4 pF when the die size increases from 1 mm x 1 mm to 4 mm x 4 mm. Similarly, the peak current increases together with the source capacitance. In this calculated event the rise time is from 10 ps to 22 ps depending on the source capacitance and location of the contact point. Here, the peak current and rise time depend on the discharge path series resistance, series inductance, and physical frequency response of the 3D setup. Real designs can have different current waveforms due to a more complex die construction and varying contact resistances. This example represents discharges from a small die with low contact resistance.

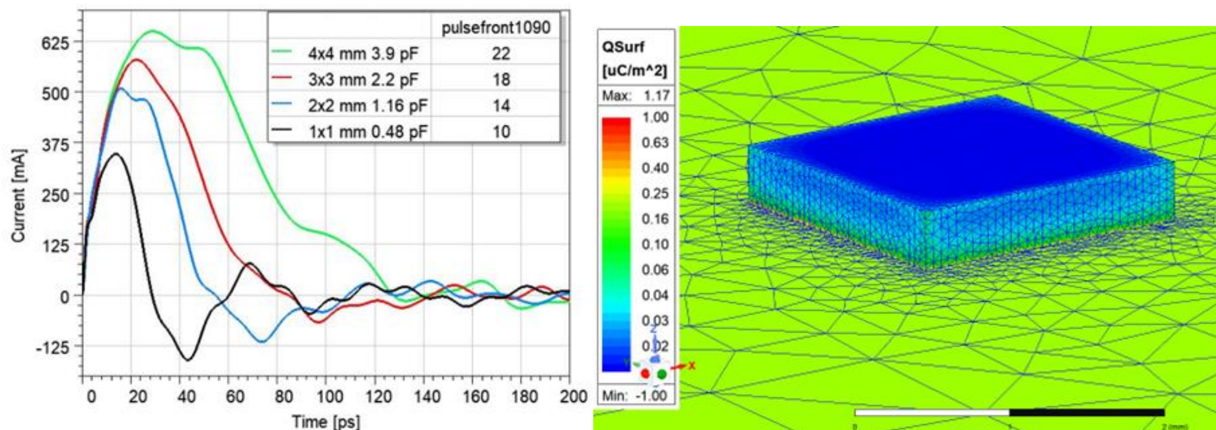


Figure C.1: Discharge Current Waveforms from a Charged Die

Note: 3D simulation model on the right side with initial charge distribution and mesh structure plotted on surfaces.

In Figure C.2, a 7 mm x 7 mm IC is placed on top of a larger 28 mm x 28 mm IC by a nozzle. Here both components have a die, bond wires, an interposer, and micro ball grid array connections. The die in the middle of the 7 mm x 7 mm IC is simplified as an aluminum block. The discharge point (white arrow) between the two ICs is in the middle of the edge of the smaller IC, the series inductance is 5 pH, and the series resistance of the discharge path is varied between 1 Ω and 13 Ω. The calculated discharge current has an initial short pulse from the charge stored on the 2.5 mm long bond wire and interposer structure. The main pulse of the discharge current flows after 10 ps through an on-chip protection circuit. In this case, the pulse rise time of 70 ps to 100 ps is longer due to the extra inductance from the IC package if compared to the previous more simplified ideal D2D discharge event.

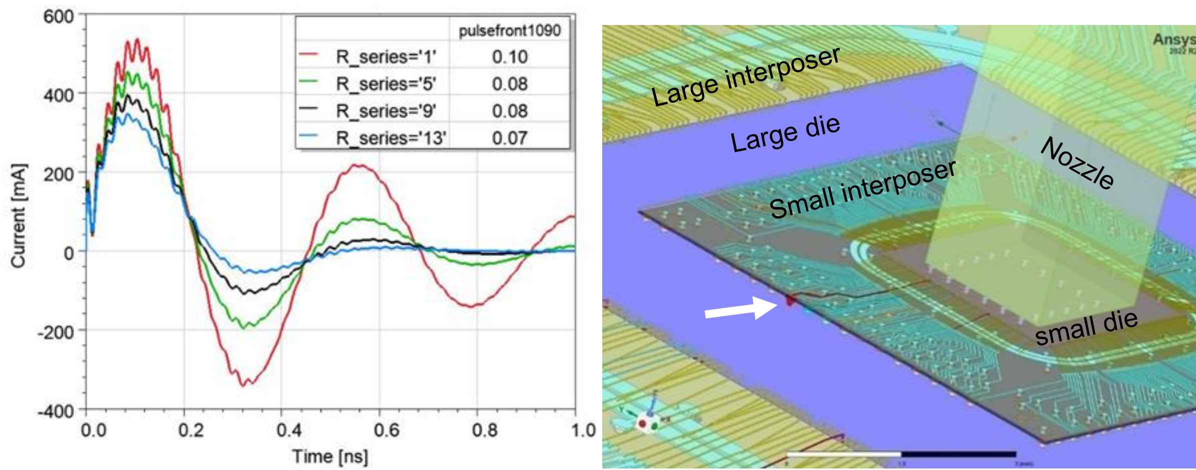


Figure C.2: Discharge Current between Two ICs with Varying Discharge Path Series Resistance

Figure C.3 presents the third type of discharge scenario. Here the die is 4 mm x 4 mm in size but now the initial discharge voltage is 3 V, and the contact resistance is high enough to produce an overdamped discharge current waveform. In this scenario, the series inductance is close to zero, thus, providing rapid initial current rise times from a 4-pF source. This can be a realistic ESD event when the die voltage decreases as it approaches another conductor, and surfaces have oxidation or other materials with limited conductivity.

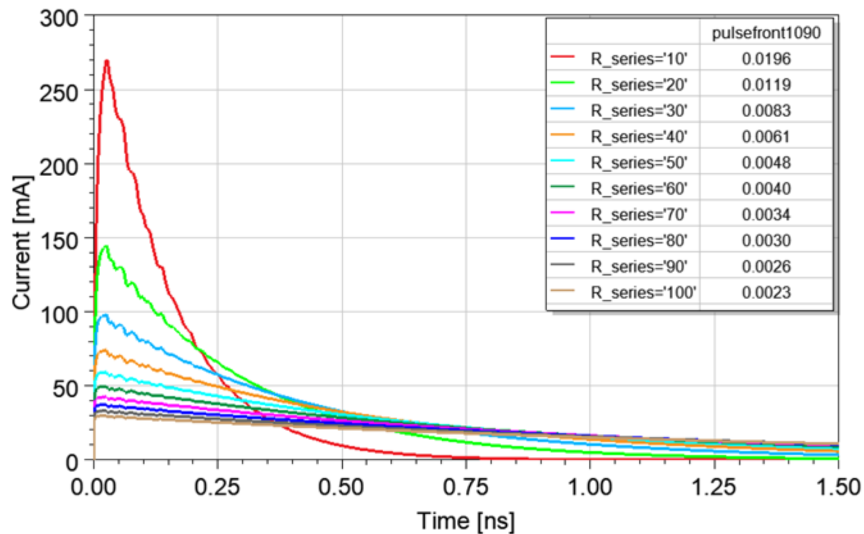


Figure C.3: Discharge Current between Two ICs with Varying Discharge Path Series Resistance

Based on simulations any of these three discharge scenarios can in principle exist and the main challenge is to estimate the final discharge voltage and contact resistance. The exact discharge current waveform calculation requires detailed knowledge of the die or IC structure, information on the used materials, and knowledge about the close surroundings where components are assembled physically together. If this data is available, 3D calculation tools can be used to estimate various D2D or IC-to-IC discharge scenarios and use this data to optimize the level of required on-die ESD protection.

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Revision History

Revision	Changes	Date of Release
1.0	Original release	August 2023